3-1-1991

Establishing a bipolar fabrication service for analog circuit realization at the Rochester Institute of Technology

Andrew La Pietra

ESTABLISHING A BIPOLAR FABRICATION SERVICE FOR ANALOG CIRCUIT REALIZATION AT THE ROCHESTER INSTITUTE OF TECHNOLOGY

by

Andrew R. La Pietra

A Thesis Submitted

in

Partial Fulfillment

of the

Requirements for the Degree of

MASTER OF SCIENCE

in

Electrical Engineering

Approved by:

Professor Lynn Fuller
(Thesis Advisor)

Professor _____

Professor Robert E. Pearson

Professor _____
(Department Head)

DEPARTMENT OF ELECTRICAL ENGINEERING
COLLEGE OF ENGINEERING
ROCHESTER INSTITUTE OF TECHNOLOGY
ROCHESTER, NEW YORK
MARCH, 1991

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Date 2 / 18 / 91

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ABSTRACT

A bipolar fabrication service has been developed at the Rochester Institute of Technology to service students and faculty from the Microelectronic, Electrical and Computer Engineering departments wanting to realize designed integrated circuits. The fabrication technique combined implanted N-Well and double diffusion processes.

Phosphorous was implanted into a p-type substrate, oxidized for eight hours and diffused in nitrogen for another 40 hours to create isolated n-wells. Devices were then fabricated using a double diffusion process.

The CAD tool used for the service is the Integrated Circuit Editor, ICE, which has campus wide accessibility through the RIT VAX system. Designed standard cells include resistors, bipolar and MOS transistors, a current mirror, a differential amplifier, a Darlington circuit and an operational amplifier. Full custom circuits can also be designed using ICE. Maskmaking files generated from circuit designs are sent to the Microelectronic Engineering department for circuit fabrication, and the completed circuits are returned to the designer for testing.

The RIT N-Well process has provided vertical NPN and PNP transistors with common emitter current gains of 100 and 40 respectively, Early voltages greater than 50 volts, and breakdown voltages higher than 15 volts. Differential amplifiers and current mirrors have alos been successfully designed, fabricated and tested.

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PREFACE

The RIT Bipolar Fabrication Service was established to mirror a simple production operation from inital circuit design to circuit manufacturing to final testing. To accomplish this task the project was separated into three areas: formation of a standard cell design library, fabrication process development and implementation of the service (see figure A-1). This breakdown aided in providing a structure from which to start and finish the project.

The standard cell library was developed first and was continuously enhanced as the project proceeded. The library is a collection of simple circuit designs ranging from discrete transistors to an operational amplifier. Since the turn around time from design to test was limited to one RIT quarter, the standard cell library eliminated some design time by providing pre-assembled devices. The first cells were resistors and discrete bipolar transistors, but with each process iteration more cells were added to test the fabrication process. Threre are over 50 cells in the library and consist of several resistors, bipolar and MOS transistors, and simple circuits.

The second phase of the project was the development of a working fabrication process that would produce usable and consistent results. To begin, the initial qualitative process was assigned numbers, or rather processing parameters. This process was then simuated with computer

software and the results were analyzed using device physics equations to find transistor parameters. The process was repeatedly altered and simulated to obtain the desired results. Once the process was formulated wafer processing began. As processing was completed the actual device parameters were obtained and process changes were made accordingly until an acceptable process was established (see figure A-2).

The third step in the project was the service implementation. This mainly consisted of documenting everything in a simple form, but included writing every step in the manufacturing process, collecting and organizing the standard cell library and producing a users manual. The users manual outlined design rules, processing steps, process simulations, circuit simluations, CAD information, design examples for the users and generally how the service worked. (see figure A-3).

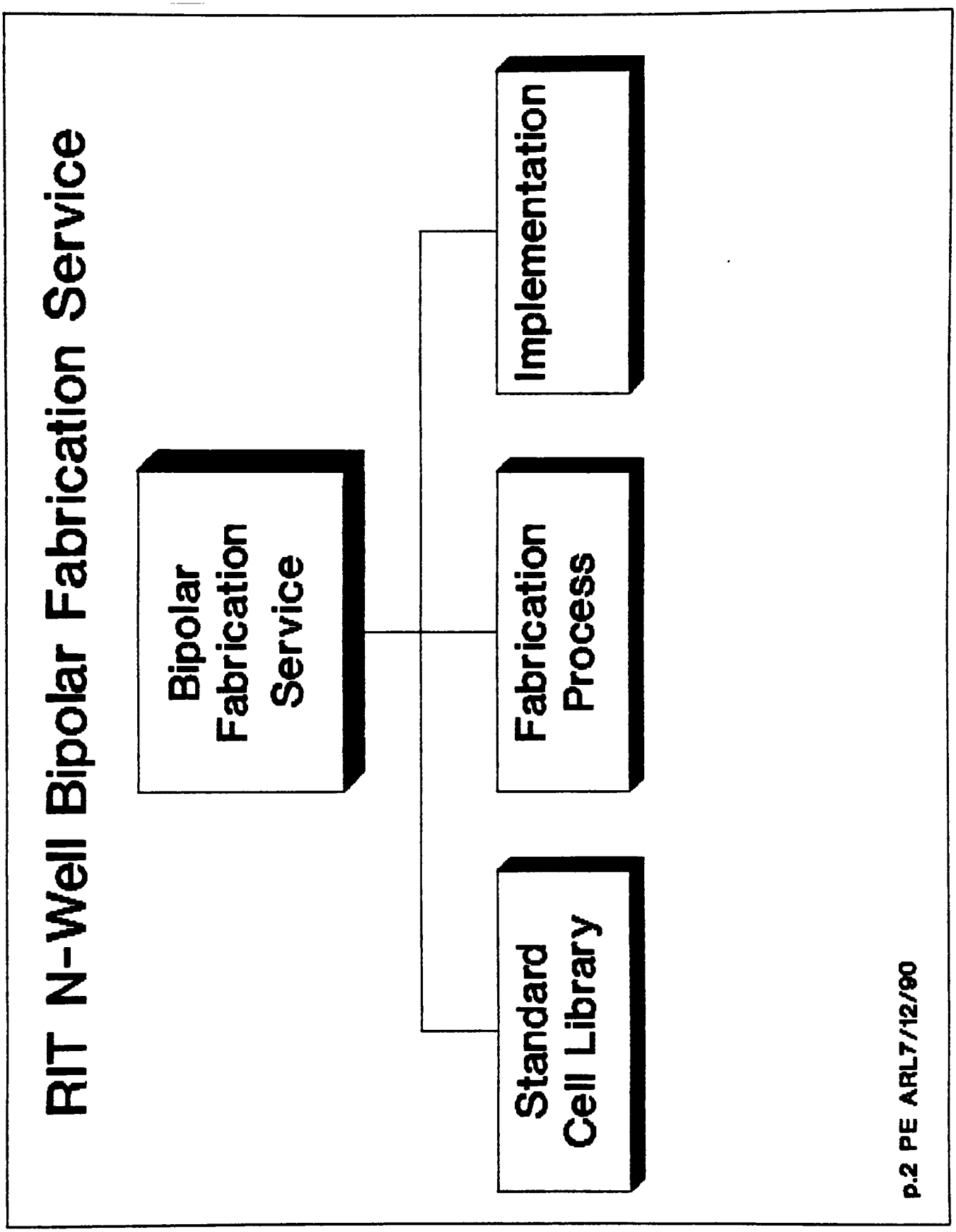

Figure A-1: Project Overview

RIT N-Well Bipolar Fabrication Service

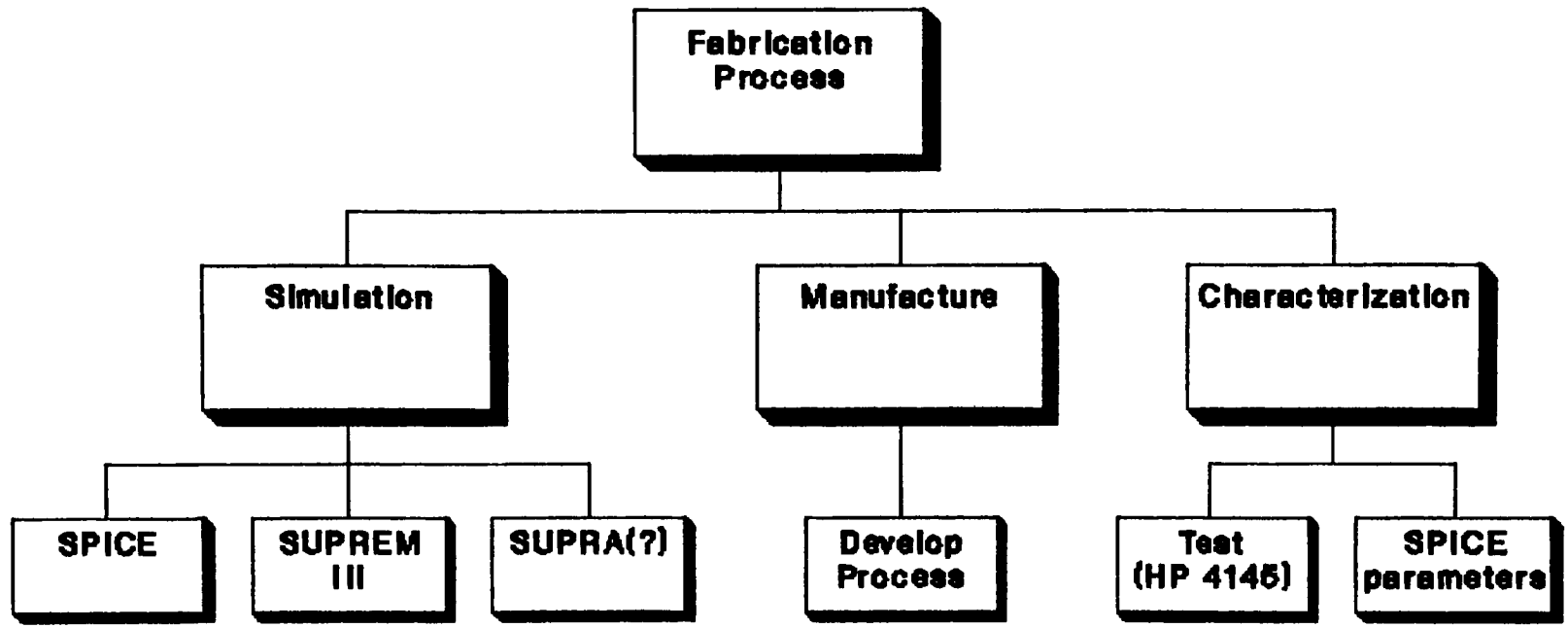

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Figure A-2: Fabrication process breakdown

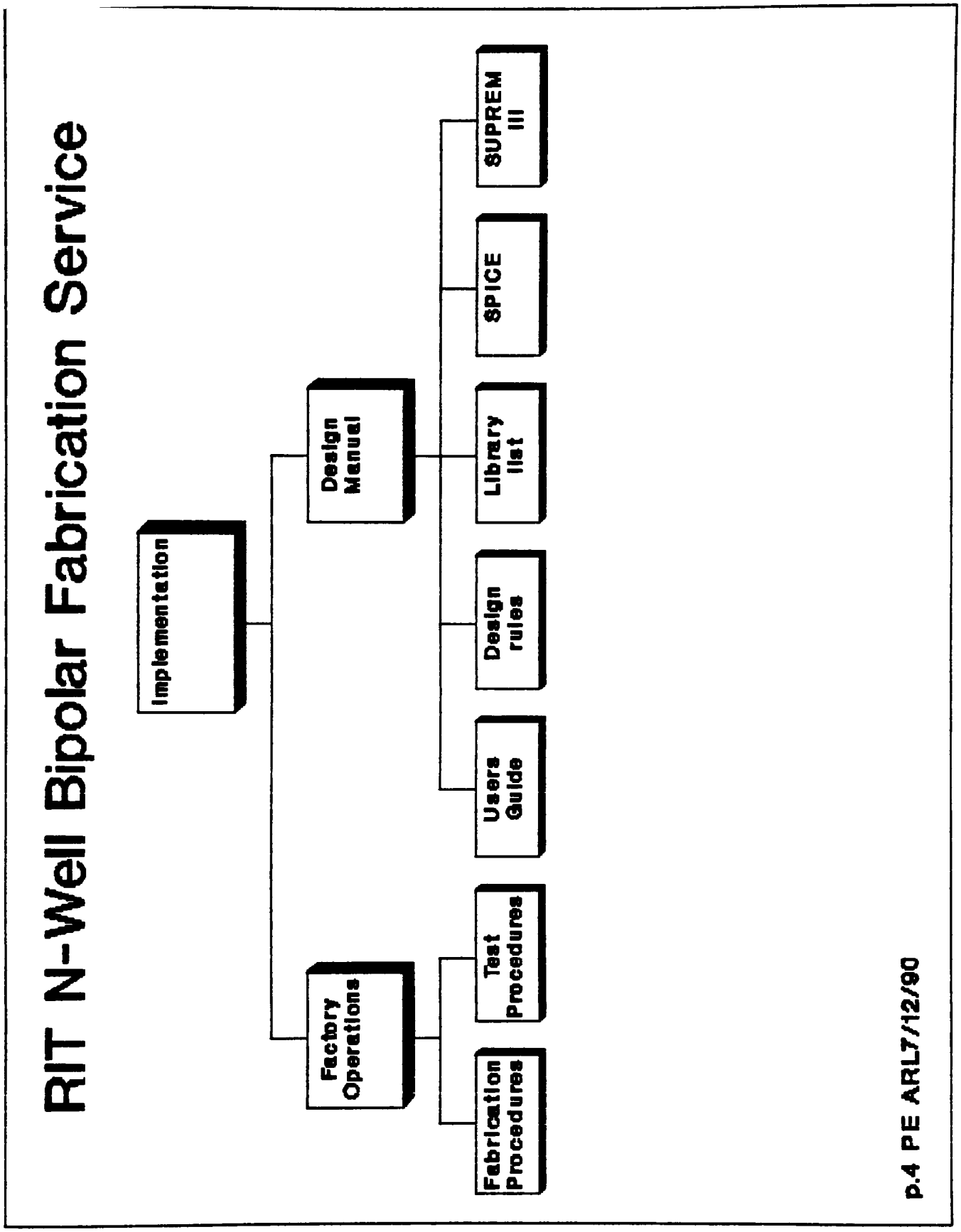


Figure A-3: Implementation

CHAPTER 1: INTRODUCTION

As semiconductor devices and circuits become more proliferate, circuit designers must become more familiar with integrated circuit (IC) design. Correspondingly, IC design techniques must be available in the educational system. At the Rochester Institute of Technology, Integrated Circuit Editor (ICE) is VAX resident software used to design ICs and is widely accessible across the campus. This allows users to design simple circuits (SSI to MSI), have them fabricated in the RIT Microelectronic Engineering Laboratories, and returned for testing. There are several digital technologies available at RIT (PMOS, NMOS, CMOS) but only one bipolar (IIL). This bipolar process is again digital, and does not provide for electrical isolation. Thus, most analog circuits are eliminated from this technology. As new IC manufacturing processes are realized at RIT's Microelectronic Engineering department, they can be used by other departments to enhance the overall education provided within the university. This is one of the major factors behind the creation of a bipolar fabrication service at RIT. Circuits can be fabricated and tested by the designers, which introduces an additional facet to the traditional circuit design classes and associated projects.

The initial idea, as seen by Dr. Lynn Fuller, was to create a fabrication process for analog circuit designs. The designs would be generated primarily by RIT students and faculty from the Electrical, Microelectronic and Computer

Engineering departments using a simple CAD tool. The layouts would be converted into masks and the circuits fabricated by the RIT Microelectronic Engineering Factory using a triple diffusion process. The process has no buried layer, but does provide electrically isolated circuits. The finished product would then be sent back to the designer for testing, thus completing the cycle.

The service has three basic parts: design, fabrication and testing, but the details are more involved (See Figure 1.1). The designer first obtains a design manual from the Microelectronic Engineering department. The manual is a guide for the bipolar fabrication service that includes design layout rules, the fabrication and factory process steps, SUPREM III results, a library of standard cells, SPICE simulations, device physics results.

Once the manual is procured, the circuit is given a physical layout using ICE and the provided design rules. ICE runs on the VAX which allows for campus wide accessibility to service users. ICE uses Caltech Intermediate Format (CIF) to store layout box locations, which can be converted into MANN format. Since MANN files are used by the mask generation equipment, any tool that can produce MANN format can be used with the bipolar fabrication service. The MANN files are submitted to the Microelectronic Engineering Factory, and five to six weeks later the finished devices are returned, in wafer form, to the designer. At this point the designer performs the electrical testing.

RIT N-WELL BIPOLAR SERVICE
FABRICATION SEQUENCE

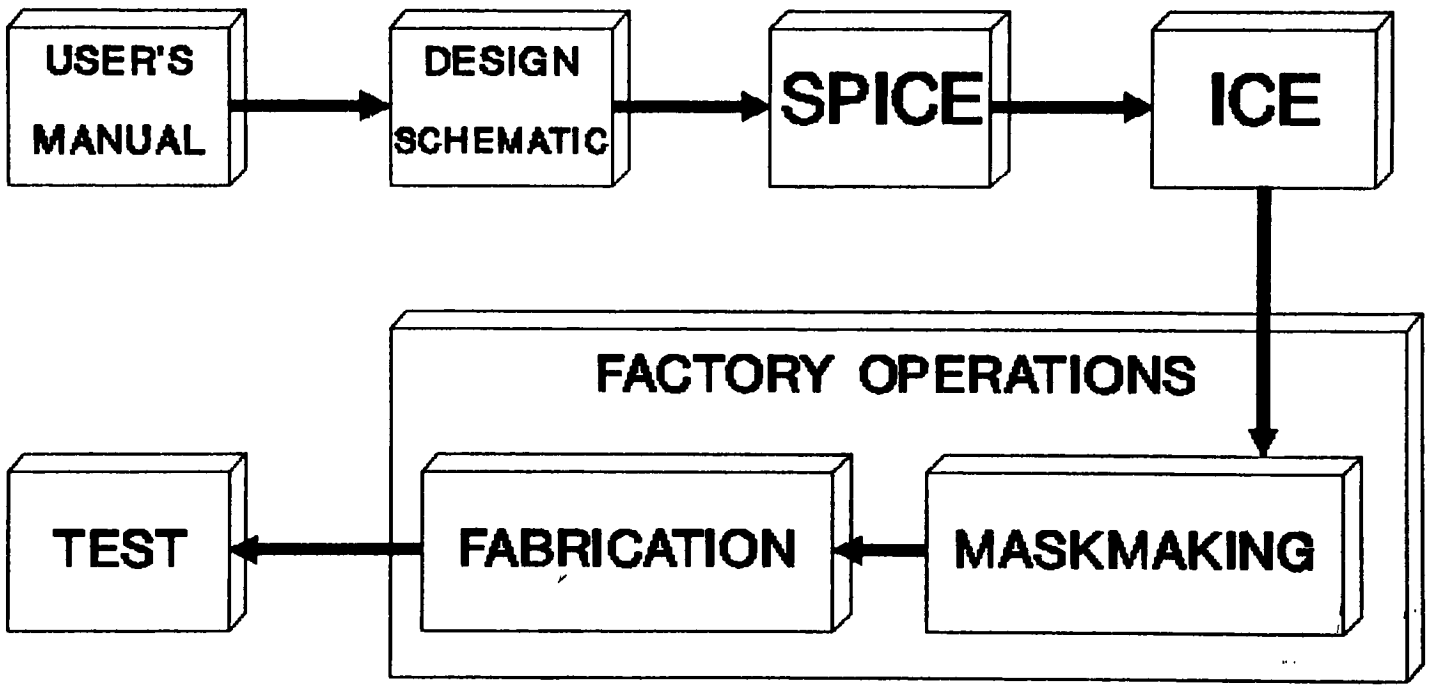


Figure 1.1: RIT bipolar fabrication service process

The RIT bipolar fabrication service can provide a wide array of silicon-based devices and circuits to the designer. They include vertical NPN and PNP bipolar junction transistors, lateral NPN and PNP BJT's, diffused resistors, JFETS, PMOSFETS, NMOSFETS and capacitors. Available in the standard cell library are simple circuits including a Darlington pair, a differential amplifier, a current mirror and an operational amplifier. The design area is 4000 microns by 4000 microns and uses a minimum geometry of 10 microns. These large geometries are an attempt to compensate for the low transistor current flow due to the absence of a buried layer. While the main target for the service was analog design fabrication, digital circuitry such as IIL, ECL, and TTL can be fabricated as well.

CHAPTER 2: THE RIT N-WELL FABRICATION PROCESS

The RIT isolated N-well Bipolar Process is a triple diffusion process employing five lithography levels. The first diffusion establishes an electrically isolated n-type well inside which the working devices are fabricated. The next two lithography steps define the p-type base and the n-type emitter for a vertical NPN transistor. The fourth lithography marks the contact cut windows and the fifth patterns the metal traces. The process is laid out graphically in detail throughout this chapter. The process specifics are in the factory process found in Appendix 2.1.

The starting wafer is a high resistivity (5 - 15 ohm-cm) p-type (boron) substrate with (100) crystalline orientation. The low initial doping level is required since subsequent diffusion must yield impurity concentrations higher than the starting level. A p-type substrate is used since it allows isolated NPN transistors to be fabricated, and these devices are of primary interest to analog circuit designers. The (100) crystallographic orientation permits slower diffusion and oxidation steps which enhances process control, see Figure 2.1.

GETTERING (Optional)

At this point the wafers can be gettered (see Figure 2.2). Many types of unwanted impurities are removed from the wafer's device areas by trapping them in crystalline defects.

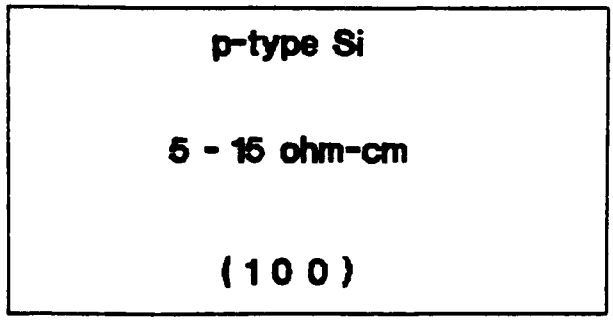


Figure 2.1: The starting wafer

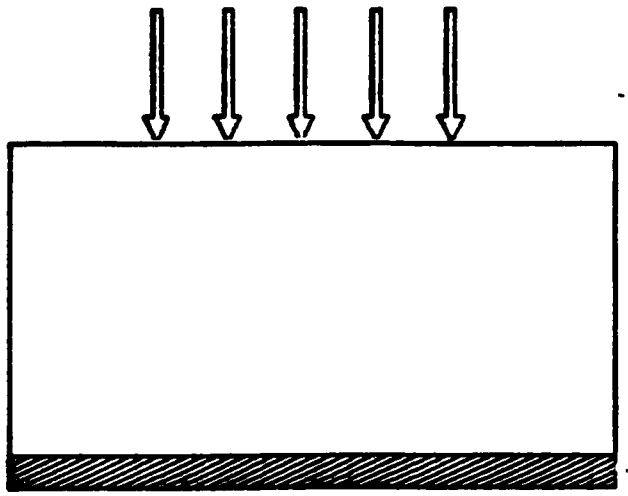


Figure 2.2: Backside gettering

Because the crystalline defects represent a lower energy state to the impurities, defects move to these states and lose the energy required to move about the wafer[1].

In the RIT N-Well process, spin-on n-type dopant is applied to the back of the wafers via manual spin coating. As the process continues, the n-dopant diffuses into the back of the wafer and perturbs the crystalline structure to create impurity traps. After the spin-on dopant is applied, it is diffused into the wafers by an 1100^{o}C bake in nitrogen (N_2) for 30 minutes.

THE N-WELL FORMATION

The N-Well formation is the first major process sequence. The first oxide growth (Figure 2.3) has two purposes. First, it removes surface damage by trapping it in the silicon dioxide (SiO_2). Second, it creates a layer used to mask the first diffusion (Figure 2.34). The first photolithography uses a standard HMDS/Positive photoresist coating that is exposed using a contact aligner, as are all the lithography exposure steps.

Once the first resist mask is developed, the SiO_2 beneath the resist is etched in 1:1 hydrofluoric acid/ deionized water to open windows to the silicon substrate. The wafers are then implanted with an 8 x 10^{12} atoms/cm^2 phosphorous dose at a 110 Kev implant energy. The photoresist and silicon dioxide areas prevent phosphorous dopant from implanting except in the open areas. Graph 3.1

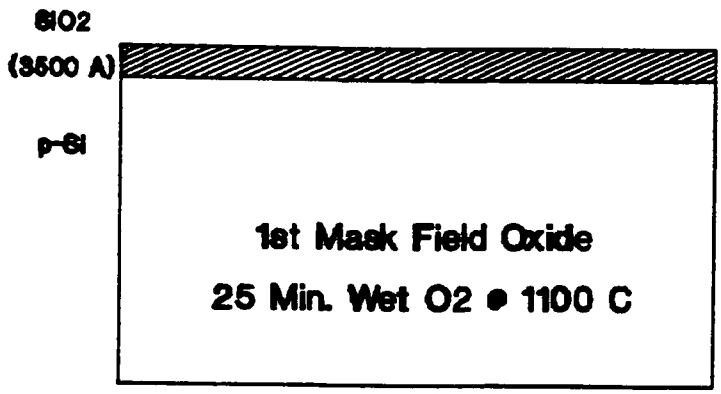


Figure 2.3: N-Well oxide formation

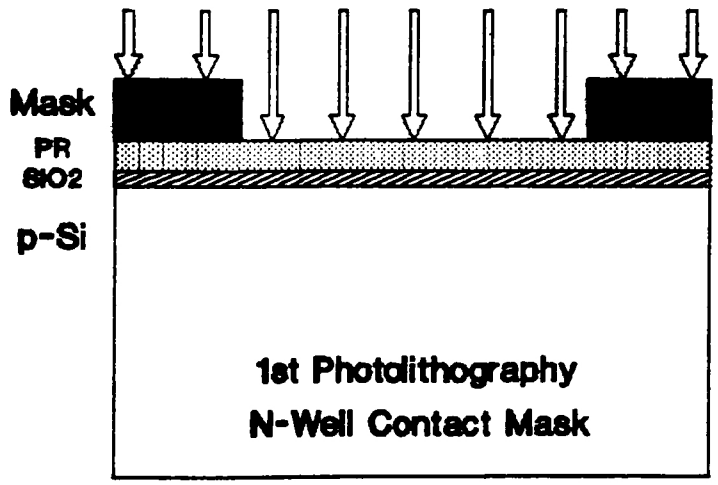


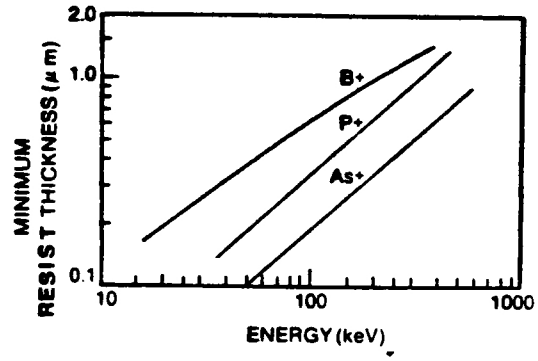
Figure 2.4: N-Well lithography

shows the photoresist thickness required to halt phosphorous ions in masked areas[1]. The photoresist is usually removed from the wafer after the SiO_2 is etched, but here it is crucial to leave the resist since SiO_2 alone will not properly mask implanted dopant. Once the implant step is complete, the photoresist is removed because the initial n-type well has been formed.

The n-type impurities introduced to the wafer by the implantation are driven deep into the p-type substrate during a long high temperature step. For eight hours the wafers are placed in an oxygen-rich 1150°C furnace with steam flowing through it. This does two things: it anneals any damage caused by the implant step and "grows" an SiO_2 layer for the base diffusion mask. Using steam provides a thicker oxide layer by increasing the initial oxide growth rate. The eight hour oxide growth is followed by a 40 hour diffusion in a nitrogen-rich ambient, again at 1150°C (see figures 2.5a and 2.5b). The resultant depth of the pn junction is approximately nine microns. Initial N-Well formation work was done by another student and is only slightly modified for this process[2].

THE BASE DIFFUSION

The next major section in the process is the base diffusion. First, the SiO_2 thickness is checked with graph 2.2 to see if it properly masks a boron diffusion cycle[1]. Figure 2.6 then demonstrates the base lithography. In this



Graph 3.1: Photoresist thickness for implant masking[1]

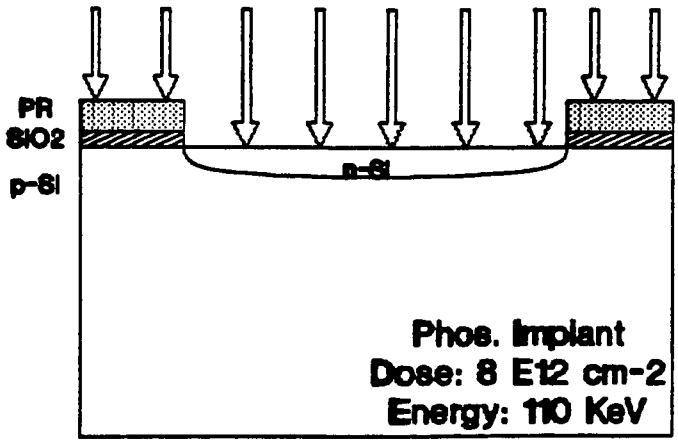


Figure 2.5a: Cross section after implant

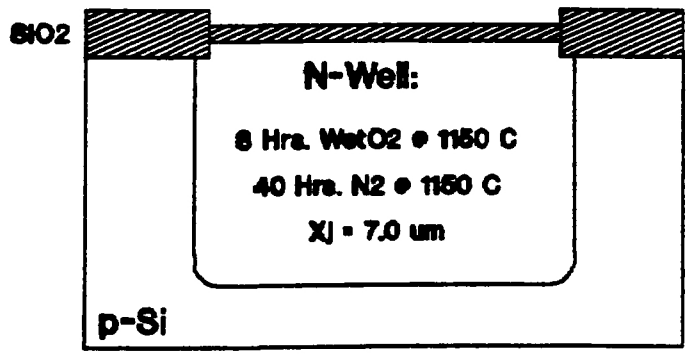


Figure 2.5b: Post-drive N-Well depth

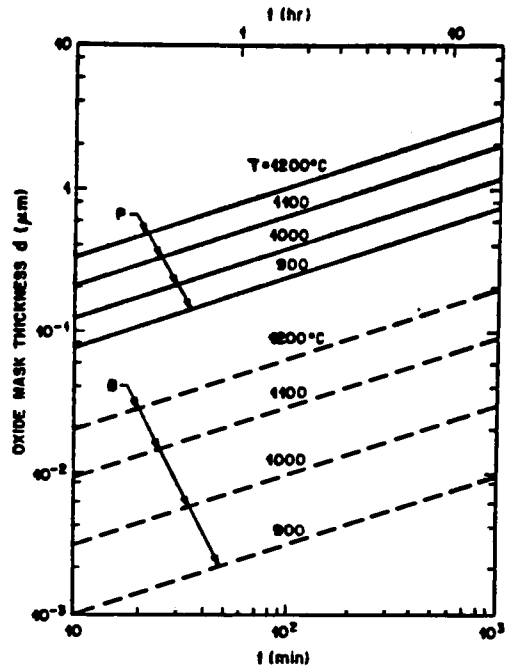
lithography step diffusion windows are etched. The photoresist is then removed by an oxygen plasma asher before the actual diffusion occurs. (The photoresist melts above 140°C and if not removed would result in furnace and wafer contamination.)

The actual base diffusion consists of three steps: the predeposition, the Boro-silicate glass (BSG) removal and the drive-in. The dopant source is a solid ceramic disk of boron nitride that, at high temperature in the presence of O_2, forms a B_2O_3 glass that vaporizes and condenses on the silicon substrate. Equation 2.1 shows the chemical reaction for this process[3].

Eq. 2.1 $$4\ BN + 3\ O_2 \xrightarrow{heat} 2\ B_2O_3 + 2\ N_2 \xrightarrow{heat} B_2O_3\ (v)$$

The solid sources are activated before being used in predeposition. The four hour activation at 800°C removes any surface moisture and introduces the B_2O_3 glass layer on the disks. The activation procedure can be found in Appendix 2.2.

The actual predeposition cycle is a controlled deposition process. The wafers are placed back to back so that each polished side faces a solid source. The boat of wafers and disks is then pushed into an 800°C furnace. From there the furnace temperature is ramped up to the deposition temperature (950°C) at 5°C per minute. A small amount of



Graph 2.2: SiO_2 thickness required for Boron masking[1]

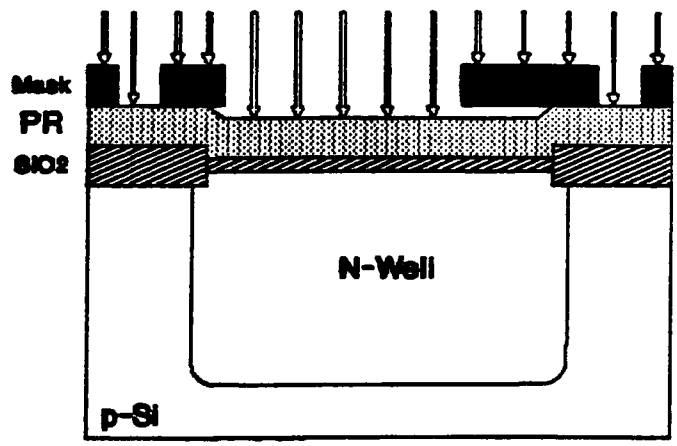


Figure 2.6: The Base lithography

hydrogen is injected into the furnace tube to enhance the B_2O_3 formation, and the wafers are soaked at the deposition temperature for 10 minutes (see Figure 2.7). No deposition occurs below 900°C and the slow process allows for uniform and repeatable results.

Once the predeposition is complete the BSG layer is removed. This is not trivial since boro-silicon-dioxide compounds do not etch easily in hydrofluoric acid (HF). Any SiO2 formed during predeposition is removed in a 10:1 H_2O/HF solution. This is followed by a low temperature SiO_2 formation (750°C for 25 minutes in wet O_2), which breaks up the BSG as oxygen diffuses through it to the silicon surface[3]. Once the BSG is loosened it is removed with a 10:1 dilute HF solution as before so as not to remove all of the field oxide. The process is shown graphically in Figures 2.8a, 2.8b and 2.8c.

The final step in the base diffusion cycle is the drive-in. The drive-in distributes the p-type dopant inside the N-Well and allows room for an n-type emitter inside the p-type base diffusion. The base drive-in also forms an SiO_2 layer which helps lower the amount of boron dopant to a desired level and forms the third lithography masking layer. The drive-in is an SiO_2 growth in wet O_2 at 1100°C for 30 minutes followed by a 20 minute dry O_2 growth at 1150°C (Figure 2.9).

In Figure 2.9 the p_+ regions outside the N-Well serve two purposes. First, they prevent the substrate from being depleted of boron at the surface. If this were to happen

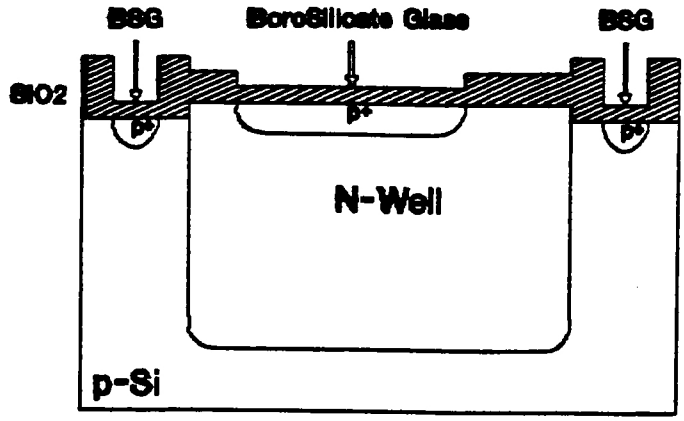


Figure 2.7: The base predeposition

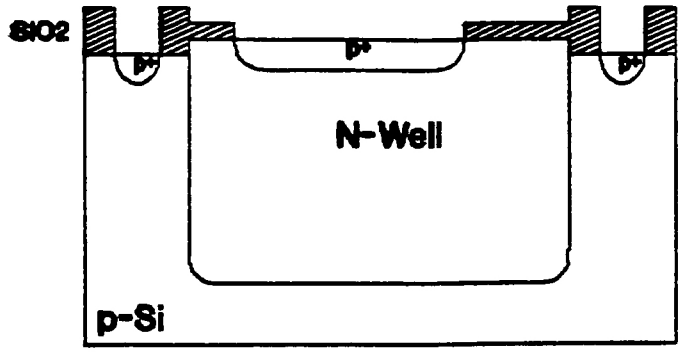


Figure 2.8a: The initial base oxide removal

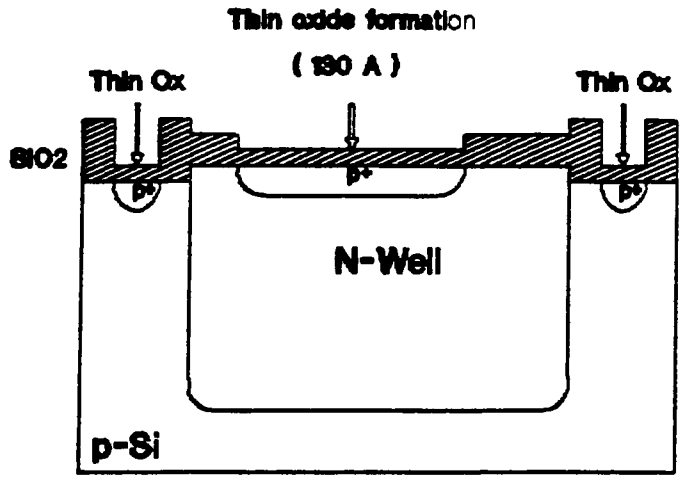


Figure 2.8b: Low temperature oxide for BSG removal

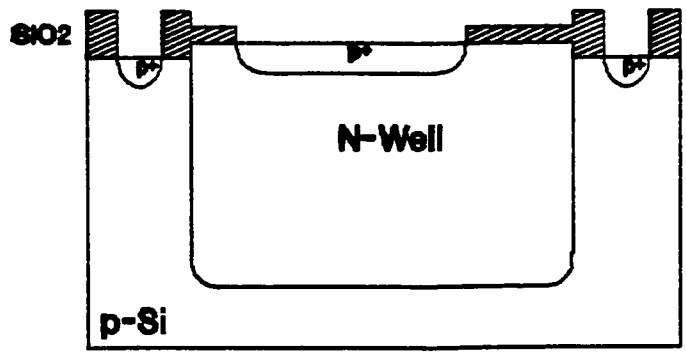


Figure 2.8c: The final BSG removal

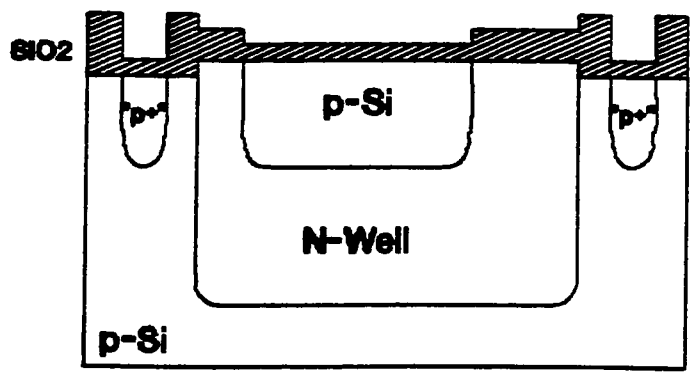


Figure 2.9: The base drive-in

then parasitic depletion-mode NMOS transistors would form between adjacent wells because the p surface would be depleted of carriers making it appear as an n-type area. Second, the electrons that escape from a well are drawn to the p-region and prevent parasitic lateral NPN transistors from being formed.

THE EMITTER DEPOSITION

To begin the emitter deposition cycle the SiO_2 thickness is checked on Graph 2.2 to make sure it properly masks diffusing phosphorous. The emitter diffusion windows are formed in the same manner as the base diffusion windows, but with the third mask in the process (see Figure 2.10).

Again a ceramic solid source is used as the dopant source, and the deposition cycle is similar to the base diffusion. The activation step is a four hour dehydration at $800^{o}C$. Next, the wafers and disks are loaded into an $800^{o}C$ furnace, ramped up to the deposition temperature ($975^{o}C$) at $5^{o}C$ per minute, soaked at deposition temperature (20 minutes) and ramped down to $800^{o}C$. During the process the phosphorous breaks down into vaporous P_2O_5 which deposits onto the silicon wafers. The deposition chemistry is described in equation 2.2, and the deposition cross-section is described in figure 2.11.

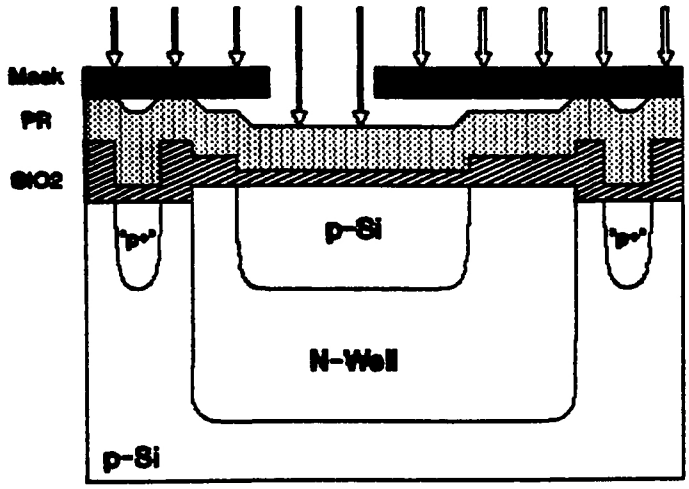


Figure 2.10: The emitter lithography

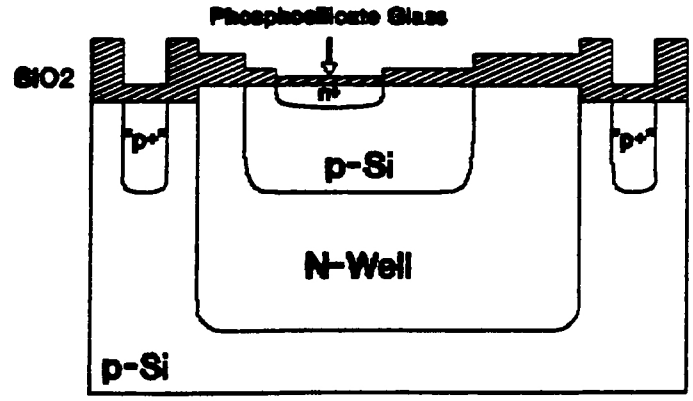


Figure 2.11: The emitter predeposition

Eq. 2.2 $$SiP_2O_7 \xrightarrow{\text{heat}} P_2O_5\ (v) + SiO_2$$

No oxygen is added to the cycle because there is sufficient oxygen in the diffusion tube for the reaction to occur[3].

At this point all SiO_2 is stripped from the wafers, and the newly formed transistors are tested for BETA (see Chapter 3), the common-emitter circuit current gain. The BETA measurement provides an idea of how long a drive-in is necessary. A typical gain for a vertical NPN transistor at this point is 15, and a sample curve is shown in Figure 2.12. For this process the emitter drive-in step is approximately 20 minutes in wet O2 at 1050°C (see figure 2.13). Again the drive-in step forms a masking layer for the next lithography.

CONTACT CUT LITHOGRAPHY AND ALUMINUM DEPOSITION

The fourth lithography defines contact windows in the emitter drive-in oxide that are used as metal connection pathways to all areas of the transistor (see Figure 2.14). When this is complete, aluminum is evaporated onto the wafers which are subsequently patterned by the fifth lithography sequence (see Figures 2.15a, 2.15b and 2.15c). Once patterned, the wafers are sintered at 450°C for 20 minutes in forming gas (H_2N_2). The sintering step alloys the silicon and aluminum to form a better electrical contact. The forming gas eliminates surface states that are sensitive to

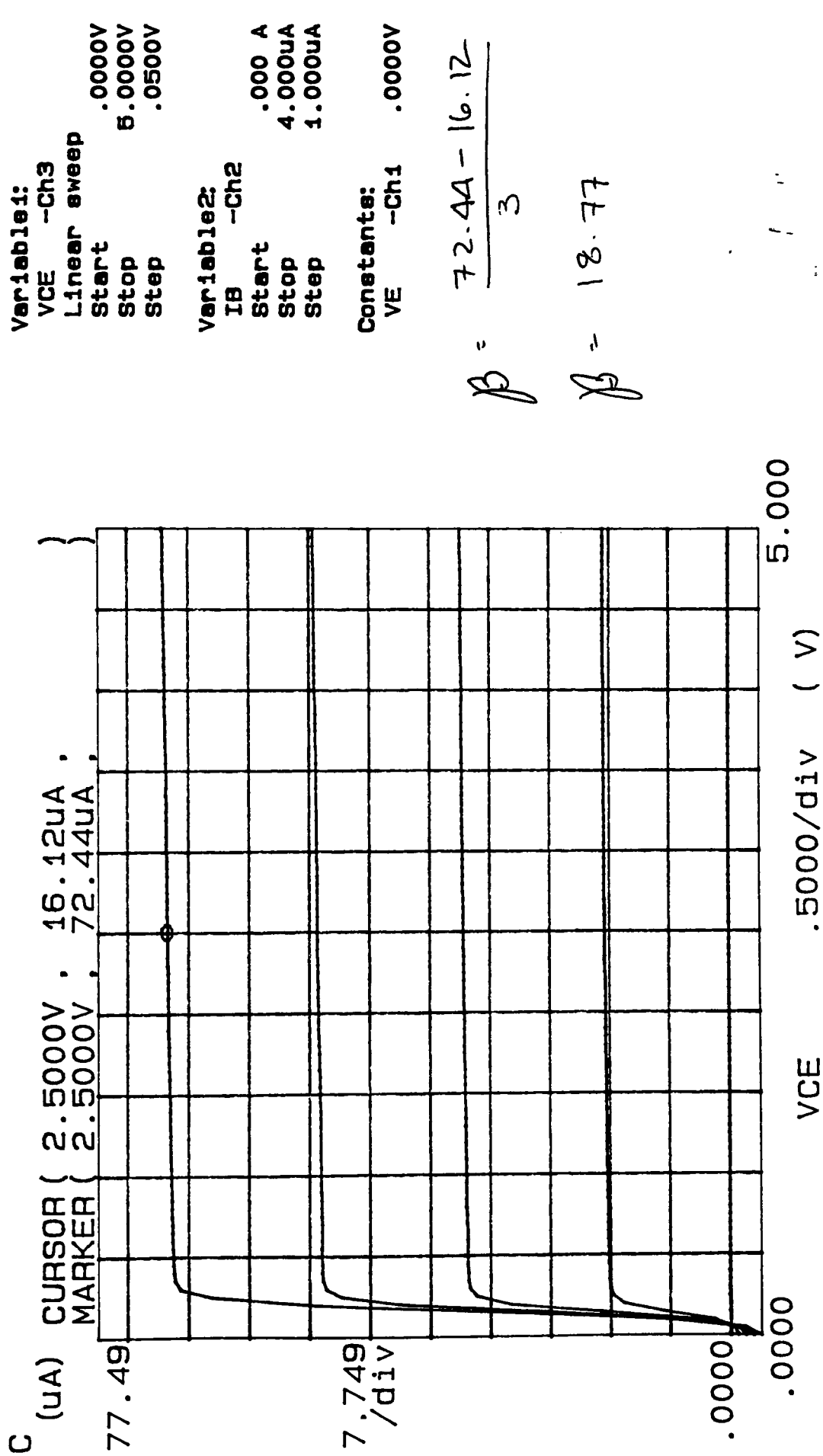


Figure 2.12: A typical transistor characteristic before emitter drive-in

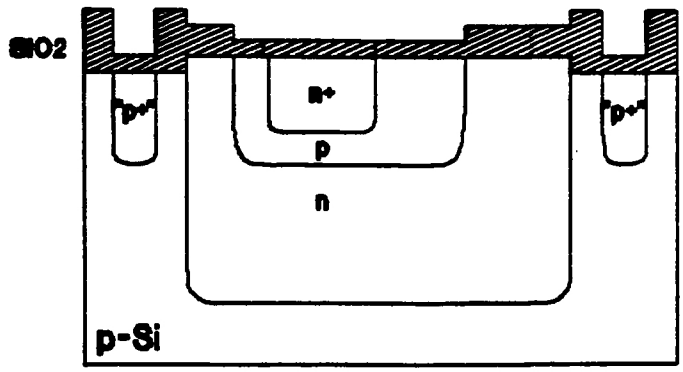


Figure 2.13: Emitter drive-in

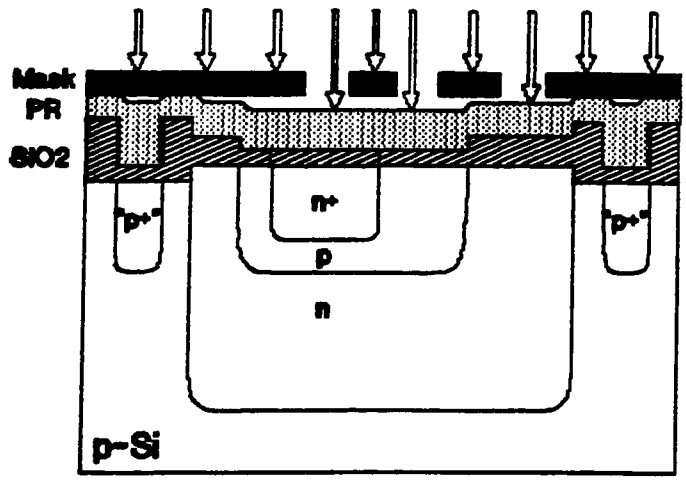


Figure 2.14: Contact cut lithography

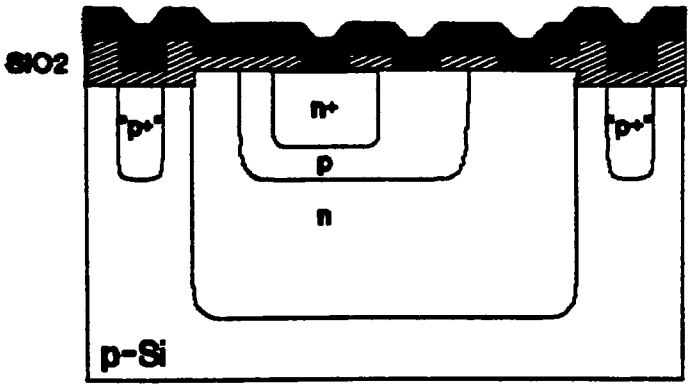


Figure 2.15a: Aluminum evaporation

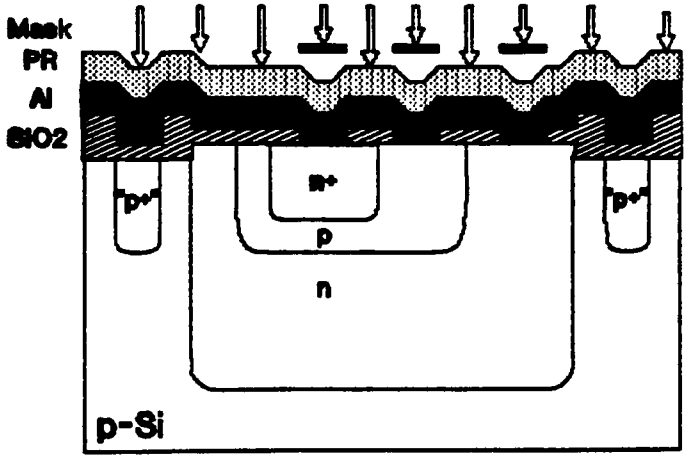


Figure 2.15b: Aluminum patterning

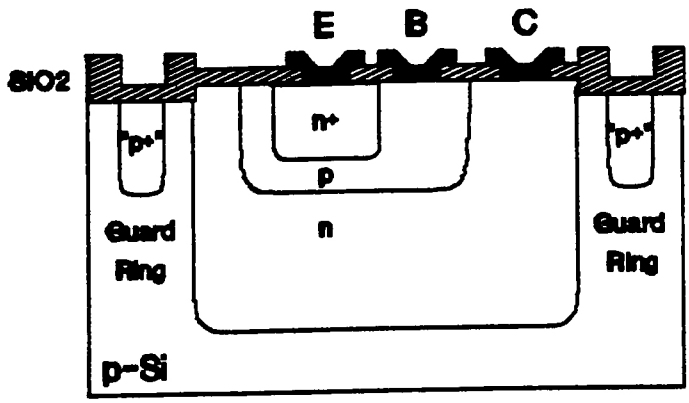


Figure 2.15c: Final structure

light and other forms of radiation. With addition processing steps, the wafers can be passivated with SiO2 should surface leakage become a problem.

RESERVATIONS

The fabrication process is basically sound because it produces working transistors; however, a few issues must be addressed. First, the dopant sources for the base and emitter are ceramic solid sources. This type of dopant source is not yet modelled by SUPREM III and the only real predictability has been through experience. For example, the solid sources routinely produce a higher sheet resistance than SUPREM predicts. Second, the lack of buried layer beneath the collector limits the current flow in the devices and causes a high collector resistance. Third, two different SUPREM programs, Stanford SUPREM III and TMA SUPREM III, were used to model this process and each program gave different results. This questions seriously the process predictability without forming an empirical model for SUPREM III to use.

CHAPTER THREE: PROCESS DEVELOPMENT

The fabrication process was developed over several months with three basic tools. First, the software package SUPREM III (Stanford University Process Modelling) was used extensively to obtain target processing parameters. Second, several device physics concepts and equations utilized the SUPREM III output to find device parameters. After fabrication, an HP4145 Semiconductor Parameter Analyzer was used to test devices and circuits, and process changes were made in accordance with test results. This chapter covers only the device parameters as found from equations and SUPREM III.

The initial concept remained the same throughout the process development stages: a triple-diffusion arrangement. There are several reasons this process was chosen, the primary one being that RIT has the capability to fabricate this process. Although most isolated bipolar processes utilize a buried layer, the required epitaxy is not yet available at RIT. Under these circumstances using an epitaxial layer would have substantially increased the processing time from the target of six weeks to months, and at an additional cost of $35.00 per wafer for epitaxy from an outside vendor. Also, the triple diffusion or 3-D process needed only five masking levels[4]. This allows the student designers and fabricators to complete the process within one RIT quarter (11 weeks). Historically,the 3-D process was the

basis for more advanced bipolar technologies so it seemed logical for RIT to begin the same way.

SUPREM III, a semiconductor process modelling computer program, was used during the process development stages. The program models several types of processing steps including diffusion, etching, oxide formation, and deposition. It will produce as output junction depths, dopant concentrations, silicon dioxide thicknesses, and a host of other processing and device physics parameters[6]. SUPREM can also be modified to use empirical models specifically designed from a process and its accompanying laboratory. The dopant profiles and the electrical modelling were extensively used for the N-Well bipolar process development. A sample SUPREM output file, with corresponding impurity profile, is shown in Appendix 3.1.

The SUPREM III dopant information was used to calculate device parameters such as Beta, the common-emitter current gain, BVceo, the common emitter breakdown voltage, and several others. Also key in these calculations were the electrical simulations, which provided dopant information as the transistor simluation was "electrically biased."

Several device parameters must be considered during process development. The main parameters considered here are listed and briefly described in Table 3.1

To better understand how critical the device parameters are in defining the process it is beneficial to have a qualitative understanding of transistor operation. An NPN

Parameter	Description
BETA	Common emitter current gain
BV_{ceo}	Common emitter breakdown voltage
V_a	Early voltage
GAMMA	Emitter Injection Efficiency
$ALPHA_T$	Base Transport Factor
$ALPHA_f$	Forward ALPHA (product of GAMMA and $ALPHA_T$)
X_d	Depletion region extension
C_j	Junction capacitance
V_{bi}	Built-in voltage
J_s	Saturation current density

Table 3.1: Device parameters

transistor in the active mode is most often used so this will be described.

An NPN transistor can be viewed as two np junctions placed back to back. Figure 3.1 shows an NPN transistor biased in the active mode. The transistor acts as an amplifying switch, with the BE junction controlling the on/off operation. When this junction is forward biased, the energy barrier to majority carrier flow is reduced. As a result, the majority carrier holes on the p-side are injected across the junction into the n-side, whereas the majority electrons on the n-side are injected into the p-type base. If these injected electrons can diffuse across the p-type base before recombining with holes, a large electron current

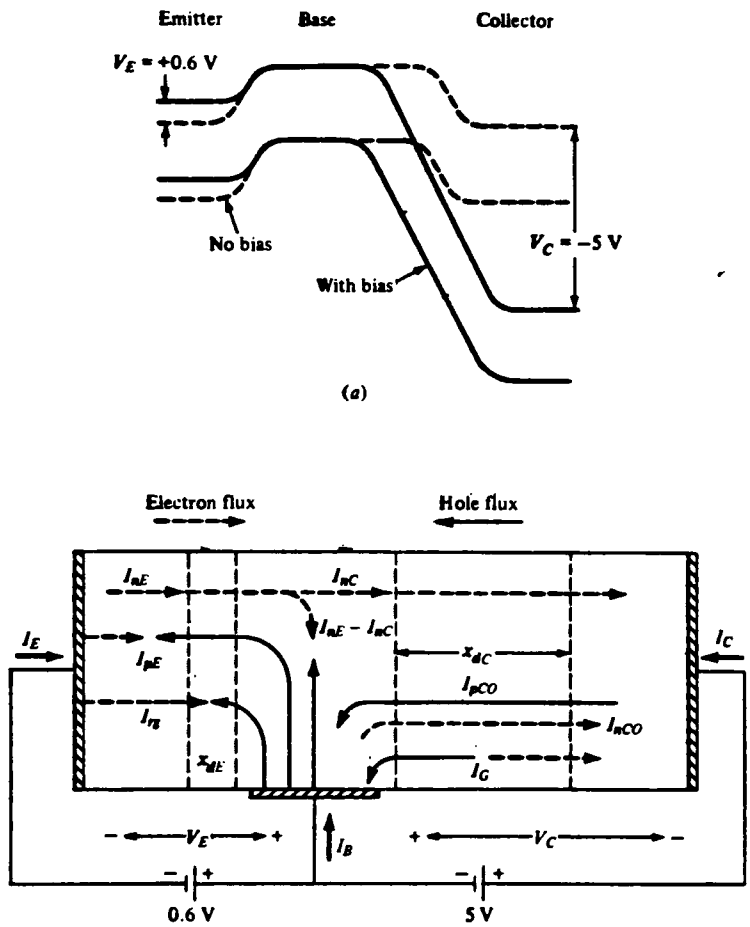


Figure 3.2: NPN transistor active mode biasing[5]

flow takes place across the collector-base junction in spite of the fact that the junction is reverse biased. The high field value created by reverse biasing this junction sweeps the electrons that reach the corresponding depletion layer straight into the second n-type region, or collector. The depletion regions surrounding both junctions are also extended into the middle p-type area, effectively shrinking the distance electrons must drift across the base. This prevents some electrons from recombining and increases the number of collected carriers[7].

To this point the desirable qualities for an NPN transistor are listed below in Table 3.2.

1. BE junction with an ideality factor close to unity.
2. CB junction that sustains large voltages before breaking down under reverse bias.
3. A base wide enough to prevent the depletion region of the CB junction from reaching through the base to the collector. This would cause the emitter and collector regions to become electrically shorted.
4. A base narrow enough so that an overwhelming majority of the injected carriers will not recombine.
5. A base doping much lower than the emitter doping to keep the amplification high by preventing back injection of holes into the emitter.

Table 3.2: List of desirable BJT qualities

In processing terms it is desirable to have a highly doped emitter, a moderately doped base and a lightly doped collector. In device design terms this translates to a high Beta, large BV_{ceo}, reasonable V_{bi}, and small leakage current.

DEVICE PHYSICS CALCULATIONS

The previously mentioned parameters were obtained from device physics equations using SUPREM III impurity profiles and calculations. A partial list of calculated parameter values is listed in Table 3.3

Parameter	Value
V_{bi}	.987 volts
GAMMA	.9942
$ALPHA_T$	.99986
$ALPHA_F$	.99405
$BETA_0$	167
$BETA_{-10}$	185
V_a	-91.33 volts
BV_{ceo}	15.1 volts
J_s	57.9 pA/cm^2

Table 3.3: Calculated device parameters

An electrical SUPREM III simulation was used to find several values. This type of simulation accounts for depletion region extension which alters the overall Gummel numbers in the three transistor regions. A Gummel number is

the number of electrically active impurities per unit area for a given doped region.[7]

Before continuing, a sample transistor is used throughout the following sections as an example to provide the reader with a physical sense of what the device calculations mean. The transistor is an NPN vertical transistor, "fabricated" with the RIT N-Well Bipolar Process via SUPREM III. The peak emitter doping is 8×10^{19} atoms/cm^3, the peak base doping is 8×10^{16} A/cm^3 and the collector doping is 8×10^{15} A/cm^3. The sample SUPREM III impurity profile is for this transistor and the full output file is located in Appendix 3.1.

Vbi (BUILT-IN VOLTAGE)

The first parameter found was the base-emitter junction built-in voltage that defines the potential barrier to current flow at zero volts across the junction.
The steep difference in carrier concentration across the junction causes carrier diffusion, or p-side holes flowing into the n-region and n-side electrons into the p-region. As carriers leave the respective regions in an attempt to create equal doping levels on both sides of the junction they leave behind a vacant and oppositely charged lattice site. This results in a field, or energy potential, forming across the junction in opposition to the diffusion of carriers. This is graphically described in Figure 3.2. This potential difference must be overcome for current to flow in the diode.

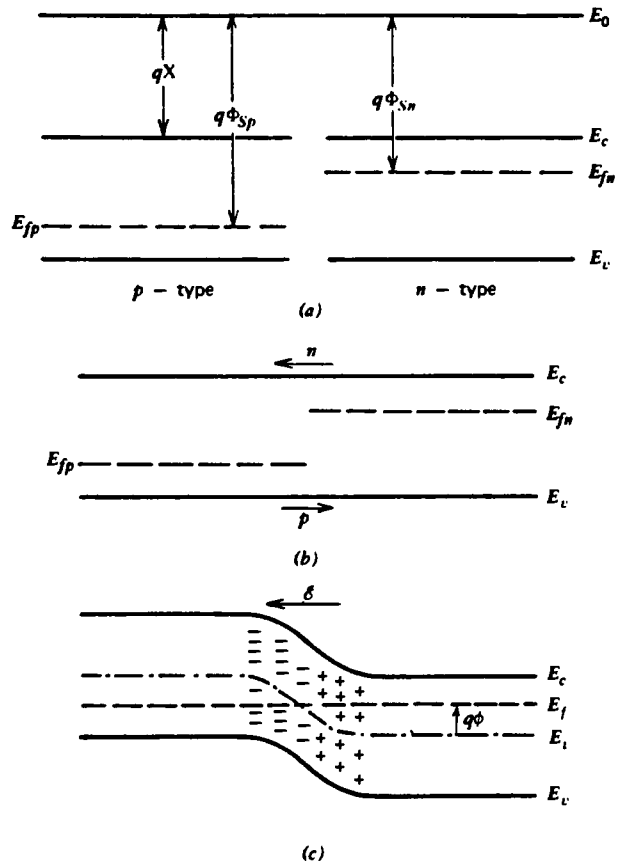


Figure 4.3 (*a*) *n*-type and *p*-type semiconductor regions separated and not in thermal equilibrium. (*b*) The two regions brought into intimate contact allowing diffusion of holes from the *p*-region and electrons from the *n*-region. (*c*) Transfer of free carriers leaves uncompensated dopant ions; these cause a field that opposes and balances the diffusion tendencies of holes and electrons.

Figure 3.2: Carrier diffusion and built-in field formation[7]

It should be noted that the standard diode assumptions are in effect[7]. The area inside this field is known as the depletion region since carriers with any type of charge are quickly swept across the field region thus depleting the region of carriers.

This potential barrier must be decreased for carriers to and current to flow. When a positive voltage is applied to the p-side of the junction within approximately 200 millivolts of the built-in potential, the diode will be forward biased and current will flow. The actual potential difference across the junction is known as the built-in voltage and is related to the junction doping levels by Equation 3.1

Eq. 3.1 $$V_{bi} = (kt/q)*\ln((N_a*N_d)/n_i^2)$$

where:
- kt/q = .026 volts at room temperature
- N_a = p-side doping level (atoms/cm^3)
- N_d = n-side doping level (atoms/cm^3)
- n_i = intrinsic carrier concentration of Si @ room temperature = 1.45×10^{10} A/cm^3

For a pn junction with $N_d = 8x10^{19}$A/cm^3 and $N_a = 8x10^{16}$A/cm^3, as obtained from a SUPREM III impurity profile, the built-in voltage is .987 volts, as listed in Table 3.3. The built-in voltages for the other two junctions were found in an

identical fashion with V_{bc} equal to .753 volts and V_{cs} equal to .662 volts.

The depletion region depth surrounding the junction is found using Equations 3.2.

Eq. 3.2 $$X_d = [2E_{si}/q((N_a+N_d)/N_aN_d)V_r]^{1/2}$$

where X_d = The depletion extension (cm)

E_{si} = permittivity of silicon

= 11.8 x 8.85 x 10-14 F/cm

q = unit of eletron charge = -1.6 x 10-19 C

V_r = Applied bias voltage on junction

= V_{bi} @ zero volts bias

The peak doping levels were used for this calculation and an abrupt junctions were assumed. For the above-mentioned junction the depletion extension is .127 um, and the majority of the extension is on the p-side due to the lighter doping.

The first requirement for active transistor operation is that the base-emitter junction is forward biased: the second condition is that the base-collector region must <u>not</u> be forward biased. If forward biasing occurred, the resulting current flow would oppose the B-E current flow and current amplification would not be possible. For calculation purposes, the B-C junction is biased at 0 volts and -10 volts because the transistor operating characteristics change as V_{bc} changes. Assuming the B-C junction is at zero volts

bias, and the B-C junction is forward biased, one can say the transistor is in the active mode based on the aforementioned criteria.

EMITTER INJECTION EFFICIENCY

The next parameter examined was GAMMA, the emitter injection efficiency. When the B-E junction becomes forward biased, opposite type carriers are injected into the base and emitter regions. The number of holes that cross the depletion region is determined by Equation 3.3 and the number of electrons that reach the base is described by Equation 3.4.

Eq. 3.3 $$p = (ni^2/N_d)\exp(V_{be}/(kt/q))$$

Eq. 3.4 $$n = (ni^2/N_a)\exp(V_{be}/(kt/q))$$

For a large BETA and small B-E junction leakage the number of holes entering the emitter, also known as back-injection, should be small, while the number of electrons entering the base should be large.

The first parameter calculated in finding the common emitter current gain is GAMMA, the emitter injection efficiency. It is a measure of the number of holes reaching the emitter versus the number of electrons reaching the base.

Eq. 3.5 $$GAMMA = [1 + (Q_b D_e/Q_e D_b)e^4]^{-1}$$

where GAMMA = Emitter injection efficiency

Q_b = Base Gummel number (atoms/cm2)

Q_e = Emitter Gummel number (A/cm2)

D_b = Hole diffusivity in emitter (cm/Sec)

D_e = Electron diffusivity in base (cm/Sec)

e^4 = Band-Gap narrowing factor

The two Gummel numbers were obtained from SUPREM III (see Appendix 3.1), and they represent the Poisson Equation solution to find the total electrical charge per unit area in a doped Silicon region[6]. The emitter Gummel number is the integral of the impurities per unit volume within the emitter depth and the base Gummel number is the integral of the impurities within the effective base width. Under low level injection conditions the emitter and base impurity levels can be approximated by the dopant levels. A quick method of estimating the Gummel number is to multiply the impurity concentration for a given region by the depth into the substrate. One must assume all doping sites are electrically active not just chemically present, and that the depth is the space that has not been overdoped with opposite type dopant.

The diffusivities were obtained from Figure 3.4 which is an impurity concentration vs. mobility/diffusivity graph[7]. The diffusivity is for injected carriers in an opposite type region, or electrons in a lighter doped p-type base for example.

The Band-Gap narrowing factor is a result of the highly doped emitter region. The high emitter doping effectively

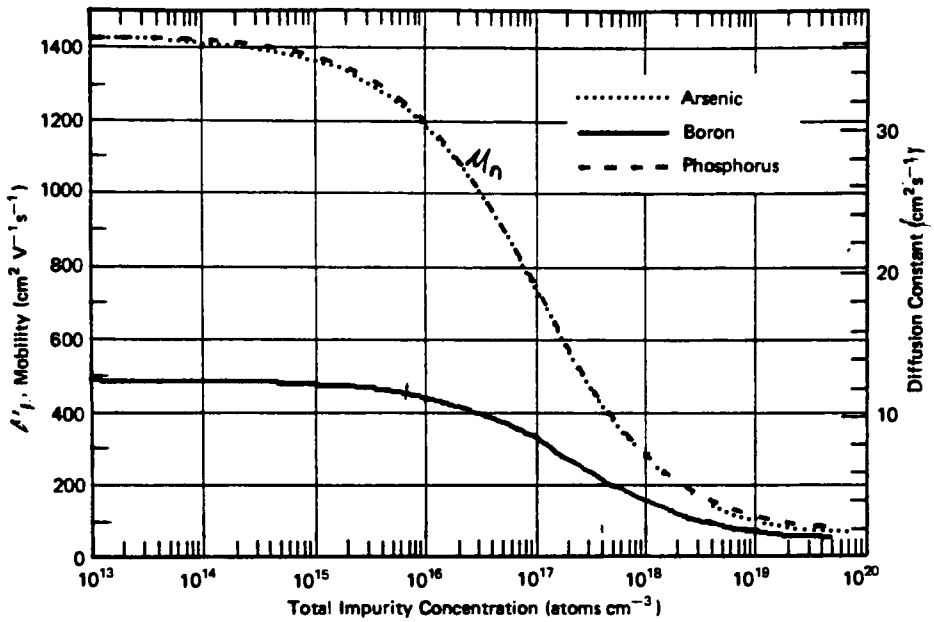


Figure 3.3: Diffusivity versus Impurity concentration[7]

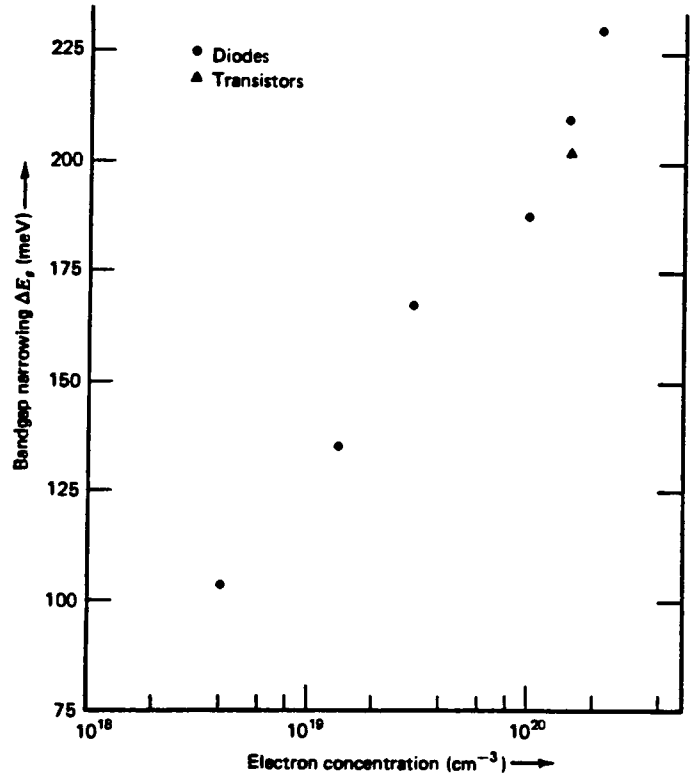


Figure 3.4:Band-gap narrowing versus Impurity concentration[7]

narrows the band-gap of silicon in the emitter because the emitter is no longer just doped silicon. The resulting phospho-silicon alloy band-gap is smaller than silicon's. As a result, less energy is required to create more free-electron carriers in the emitter and this alters the product of the free carrier densities. A more detailed description is located in section 1.1 of reference 7. In effect, it appears as though there are either more holes or fewer electrons in the emitter. As a result the free carrier density increases according to equation 3.5, and the injected carrier concentration decreases.

Eq. 3.5 $$n = (ni^2/p)\exp(\triangle E_g/(kt/q))$$

where $n = N_d$ under low level injection

p = minority carrier density in emitter

$\triangle E_g$ = Band-gap change according to fig. 3.5

kt/q = .026 volts at room temperature

The e^4 factor should properly compensate for a doping level of 8×10^{19} atoms/cm^3. An empirical graph demonstrating the band-gap narrowing with dopant levels is shown in Figure 3.5[7]. If both sides of equation 3.5 are mulitplied by the emitter junction depth, the corrected Gummel number is found. Taking all things into consideration, the sample transistor with a base Gummel number of 5.477×10^{12} A/cm^2, an emitter Gummel number of 3.841 x 1015 A/cm^2, D_{nb} = 20 cm^2/sec, D_{pe} =

1.5 cm^2/sec and a bandgap factor of e^4 produced a GAMMA of .9942 (1 is ideal).

BASE TRANSPORT FACTOR

The next parameter found was $ALPHA_T$, the base transport factor. The base transport factor measures the fraction of injected carriers that diffuse across the base and reach the collector without recombining. For narrow (less than one micron) and uniform bases, $ALPHA_T$ is close to one and is calculated using Equation 3.5. A uniformly doped base is assumed here.

Eq. 3.5 $$ALPHA_T = 1 - (X_b')^2/(2L_x) = 1 - (x_b')^2/((D_xT_x)^{1/2})$$

where $ALPHA_T$ = Base Transport Factor

X_b' = Effective base-width

L_x = Injected carrier diffusion length

D_x = Diffusivity of injected carriers in base

T_x = Minority carrier lifetime in base

The variable X_b' was found by subtracting the base side depletion region extensions of both junctions from the physical basewidth (obtained from SUPREM III). The depletion extension at zero volts will be equal on both sides of the junction, but changes as the B-C junction becomes more reversed biased. This is important since $ALPHA_T$ will increase towards one as the basewidth shrinks. This is related to injected carrier diffusion length, L_x, which is

the square root of the product of the injected carrier diffusivity, D_x, and the minority carrier lifetime, T_x, or average time before recombination.

For the sample transistor used X_b' was:

$$1.16 \text{ um} - 2(.127 \text{ um}) = .906 \text{ um}.$$

The minority carrier lifetime was taken as 10^{-7} seconds and the diffusivity was found from figure 3.4. This generated a value of .99986 for $ALPHA_T$.

ALPHA FORWARD and BETA

$ALPHA_f$, the forward common emitter current gain, is the product of the Emitter Injection Efficiency and the Base Transport Factor (see equation 3.6)

Eq. 3.6 $$ALPHA_f = GAMMA \times ALPHA_T$$

From here BETA, the DC common-emitter current gain, was found using equation 3.7 below.

Eq. 3.7 $$BETA = ALPHA_f / (1 - ALPHA_f)$$

For the sample transistor $ALPHA_f$ was .99405 and BETA was 167.

When the transistor is operating with the B-C junction deeply reversed biased, the BETA calculation is the same, but with two slight changes. First, the Gummel number for the base decreases due to a shrinking effective basewidth caused by the depletion region extension. The new Gummel number can be found by performing an electrical SUPREM III simulation

(see Appendix 3.1). Second, the base transport factor increases because there is a smaller base for injected carriers to traverse. When deeply reverse biased, the depletion extension on the B-C junction increases and is usually much greater than the B-E junction extension. With these reverse biasing considerations, BETA for the sample transistor increased to 185.

EARLY VOLTAGE

The Early voltage measures transistor operating uniformity as the collector to emitter voltage changes. In a transistor curve family all of the lines are slightly tilted. When lines are extrapolated from the saturation/linear region threshold point, or "corner," they converge to one point on the voltage axis[8]. This locates the Early voltage V_a. The curves tilt due to changes in BETA as V_{cb} biasing increases. A quick estimate of the Early voltage is shown in Equation 3.8.

Eq. 3.8 $$V_a = -(BETA_1 \; / \; (BETA_2 - BETA_1)) \times 10$$

where V_a = Early voltage

$BETA_1$ = BETA at V_{cb} = 0 volts

$BETA_2$ = BETA at V_{cb} = 10 volts

Another method can be used if the BETA values are not available. This second method uses equation 3.9.

Eq. 3.9 $$V_a = Q_b / (p(X_b) \times (dX_b/dV_{cb}))$$

where Q_b = Base Gummel number (A/cm^2)

$p(X_b)$ = Base doping concentration (A/cm^3)

dX_b/dV_{cb} = Partial differential of X_b with respect to V_{cb}

For our sample transistor, method one yielded an Early voltage of -92.78 while method two produced an Early voltage of -91.33 volts.

BREAKDOWN VOLTAGE

The transistor breaks down via avalanche multiplication when sufficient voltage is applied across the collector-base junction. The field across the junction gives free carriers enough energy to break covalent Si-Si bonds upon collisions with the semiconductor lattice. As a result, an electron and hole are free to gain energy, cause more collisions and free more carriers. The number of free carriers soon avalanches out of control, thus it's called avalanche breakdown[7]. The avalanche breakdown point can be found using Equations 3.10 and 3.11.

Eq. 3.10 $$BV_{cbo} = E_{si}[(N_a + N_d)/(2qN_aN_d)](E_{crit})^2$$

where BV_{cbo} = Collector-base breakdown voltage

E_{si} = Permittivity of silicon

E_{crit} = Field necessary to cause breakdown

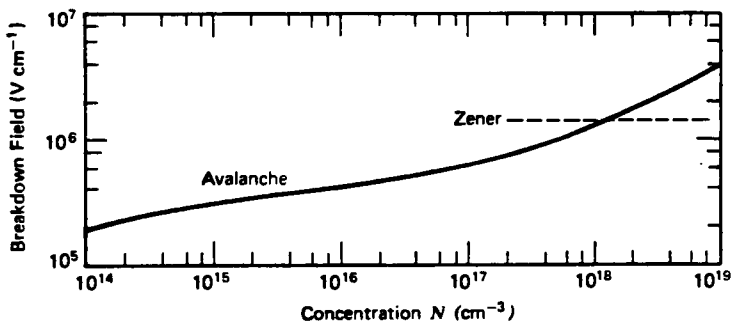


Figure 3.5: Breakdown voltage vs. impurity concentration[7]

The E_{crit} value is dependent on the lighter doped side of the junction and is found from Figure 3.5 below[7]. The breakdown of the transistor between the collector and emitter is lower than BV_{cbo} due to the transistor current gain, as shown in Equation 3.11[5].

Eq. 3.11 $$BV_{ceo} = BV_{cbo}/(BETA^{1/m})$$

where m = doping uniformity factor

For a sample transistor with base doping of 8×10^{16} A/cm^3, emitter doping of 8×10^{15} A/cm^3, BETA of 167, and m equal to four, the breakdown voltage between the emitter and collector was 15.1 volts.

A second form of transistor breakdown is known as punchthrough. This occurs when the depletion region of the C-B junction stretches through the base to the emitter and effectively shorts the transistor. If the physical base width is always larger than the maximum depletion region extension then punchthrough is prevented.

SATURATION CURRENT

The saturation current, also known as the junction leakage current, is important because it is the current that flows when the device is supposedly off. If the saturation current is too high, circuitry will not properly operate. Equation 3.12 is used to calculate the saturation current for a typical transistor.

Eq. 3.12 $$J_s = qD_xN_{xo}/X_b$$

where J_s = Saturation current density (A/cm^2)

N_{xo} = Minority carrier concentration of light doped side of junction (A/cm^3)

D_x = Minority carrier diffusivity (cm^2/s)

X_b = Base width (physical) (cm)

The saturation current density is multiplied by the junction area to find the leakage current. For the sample NPN transistor the saturation current density was 57.9 picoamps per unit area, which corresponds to a leakage current of approximately one femptoamp for a junction 40 um by 40 um.

JUNCTION CAPACITANCES

A small capacitor is usually formed whenever a depletion region is formed in a transistor. Each side of the depleted region acts as a capacitor plate, with the dielectric being silicon. When depletion regions are formed across a transistor junction, the associated capacitances are termed junction capacitances and can be calculated using Equation 3.13.

Eq. 3.13 $$C_j' = [(qE_{si}N_aN_d)/(2(N_a+N_d))]^{1/2} \times [V_{bi} + V_r]^{-1/2}$$

where C_j' = Junction capacitance per unit area

E_{si} = Permittivity of silicon

V_r = reverse bias voltage across junction

The resultant values are in Farads per unit area and can be

adapted to capacitances by multiplying by the area of a specific junction.

The sample transistor has three junction capacitances associated with it since there are three junctions. Table 3.4 below gives the calculated junction capacitances. The doping values were obtained from a SUPREM III impurity profile.

Junction	C_j/A	A_j(um)	C_j
B-E	91.95 p	40 x 40	1.471 pf
B-C	28.67 p	60 x 100	1.720 pf
C-S	16.59 p	186 x 96	2.963 pf

Table 3.4: Junction capacitance calculations

SMALL-SIGNAL MODELS

The small signal model for a transistor is highly dependent upon the DC biasing conditions established for operation. As a result, a good small-signal model was not established since the DC operating characteristics were not well defined for the transistors fabricated with this process. However, it is an important future step towards the total process characterization to form a small-signal model.

Four parameters were calculated that define a simple small signal model for an NPN transistor: the transconductance, the base-charge capacitance, the input resistance and the output resistance[8]. The transconductance was found using Equation 3.14.

Eq. 3.14 $$g_m = I_c/V_t$$

V_t is the threshold voltage (.026 volts). The base-charge capacitance, or charge storing capability in the base, was found using Equation 3.15.

Eq. 3.15 $$c_b = ((X_b)^2/2D_x)g_m$$

where c_b = Base-charge capacitance (F)
X_b = Basewidth (cm)
D_x = Diffusivity of base minority carriers (cm^2/s)
g_m = Transconductance (Amps/volt)

The input resistance was calculated using Equation 3.16.

Eq. 3.16 $$r_{in} = BETA_o/g_m$$

where r_{in} = small signal input resistance
$BETA_o$ = BETA at zero volts reverse bias
g_m = transconductance

Finally, the output resistance was calculated with Equation 3.17.

Eq. 3.17 $$r_o = V_a/I_c$$

For the sample transistor, the small signal model is shown in Figure 3.6

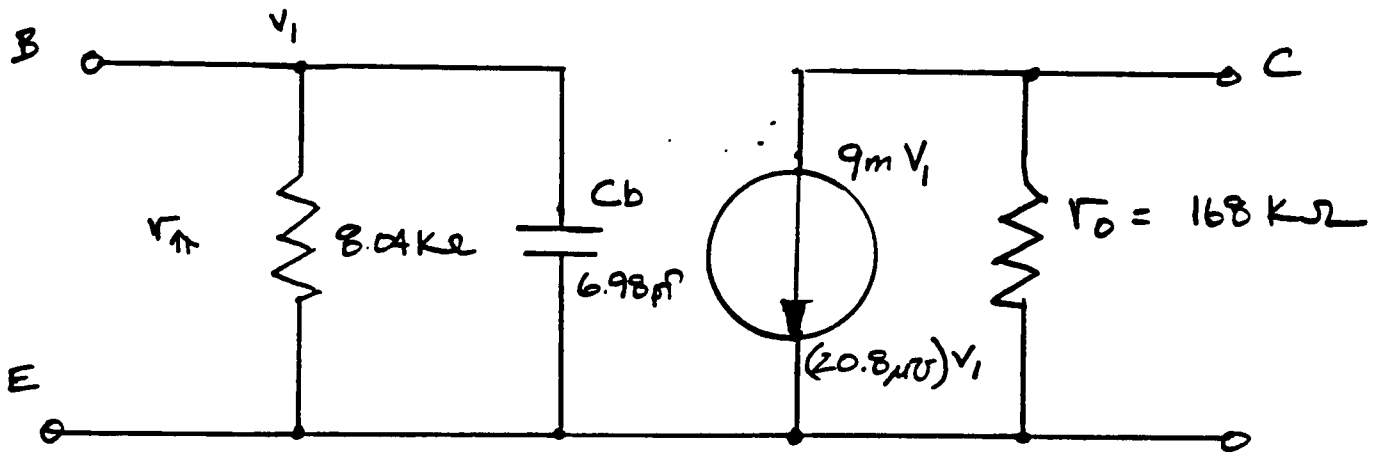


Figure 3.6: Small-signal model for sample transistor

The most important DC device operating parameters were discussed and include the gain, the breakdown voltage, the Early voltage, the saturation current, the junction capacitances and a basic small signal transistor model. As the ideas were presented calculations were made on a sample NPN transistor for example purposes. This sample transistor produced a BETA of 167, a breakdown voltage of 15 volts, an Early voltage of over -90 volts, a saturation current of 1 femptoamp, and junction capacitances in the picoamp range. A basic small signal model was formed, although the actual results are questionable, and the results are shown in Figure 3.6.

CHAPTER 4: STANDARD CELLS AND CIRCUITS

Once the fabrication process was chosen, standard cell circuitry was designed for fabrication. A list of available standard cells includes bipolar junction transistors, MOS transistors, resistors, a differential amplifier, a current mirror, an output stage, a Darlington circuit, and an operational amplifier. All designs were laid out on ICE (Integrated Circuit Editor) using 10 micron minimum geometry design rules and the RIT N-Well bipolar process (see Chapter 2).

All standard cell devices and circuits listed in the service user's manual, Appendix 4.1, were designed employing the 10 micron minimum geometry design rules also listed in appendix 4.1, as set down by Dr. Lynn Fuller, RIT Microelectronic Engineering professor. These rules were chosen for many reasons. First, the low current flow in the active devices is offset by using relatively large geometries. Second, the fabrication time is greatly reduced by using larger devices because contact aligners used in lithography are both easy to use and accessible. Third, student fabricators are allowed greater misalignment than would be allowed for five micron or smaller devices. Fourth, the process itself limits the design sizes. For example, a p-type base diffuses three microns vertically and two microns laterally. Therefore, an adjacent device must be greater than four microns away: two microns of lateral diffusion for

each device. Finally, the smallest contact cuts must be open to allow Aluminum to reach the silicon surface. The larger the contact opening design the greater the probability that it will be etched open during processing. All of these factors were taken into account when the design rules were established.

ICE

The devices and circuits were implemented into layout form using ICE, a CAD tool whose basic function is to draw boxes on a computer screen and save the box locations in Caltech Intermediate Format (CIF). Several different colors are used since each color represents a separate fabrication mask level. ICE knows which colors belong to which level by reading a process file specifically designed for a certain fabrication process, in this case the five level RIT N-Well process. The five layers as defined in ICE are N-well, base, emitter, cc (contact cut) and metal. A buried layer is also available for use with an epitaxial bipolar process. ICE is VAX resident so it provides campus wide accessibility for students and faculty using a VT240, VT340 or GIGI terminal. An ICE users manual is located in appendix 4.3 for more information.

Dr. Lynn Fuller designed the first standard cells for the RIT N-well process: a minimum geometry vertical NPN transistor, a large vertical NPN test transistor, a lateral NPN transistor and a base level resistor. Several devices

have been added to the cell library including NPN and PNP transistors, vertical and lateral, base, emitter and pinch resistors, NMOS and PMOS transistors, and several small circuits.

RESISTOR DESIGN

The base resistors were formed from the p-type diffusion located inside an N-well (see Figure 4.1). Five volts applied to the N-well and the negative five volts applied to the substrate keep the resistor isolated from other circuitry by reverse biasing the substrate-collector pn junction. Every diffusion has an associated sheet resistance that is used to design a resistor. The base sheet resistance (R_{sb}) was empirically determined from the RIT N-well process to be approximately 250 Ohms per square unit. The R_{sb} was used in Equation 4.1 to find the required diffusion length to width ratio necessary for a chosen resistor value.

Eq. 4.1 $$\text{Resistance} = L/W \times R_{sx}$$

where: L = length (in direction of current flow)

W = width (perpendicular to current flow)

R_{sx} = sheet resistance of diffusion

For example, an 18 kohm base resistor with a 250 ohm/square sheet resistance would be 720 microns long if the width were 10 microns. Large resistors requiring long lengths are folded inside N-wells, and the corner and clubhead resistances

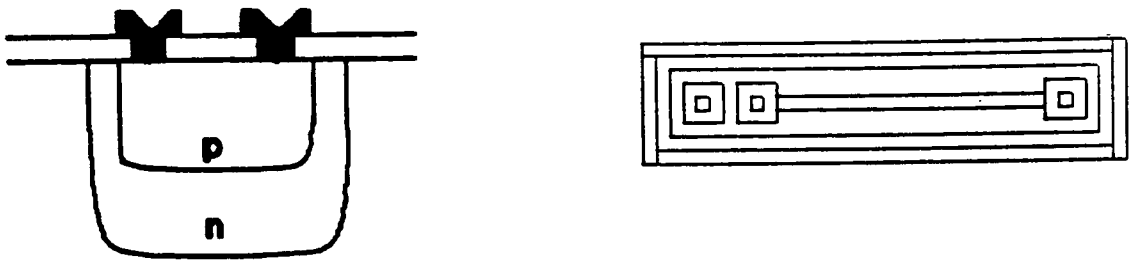


Figure 4.1: Base resistor cross-section and top view

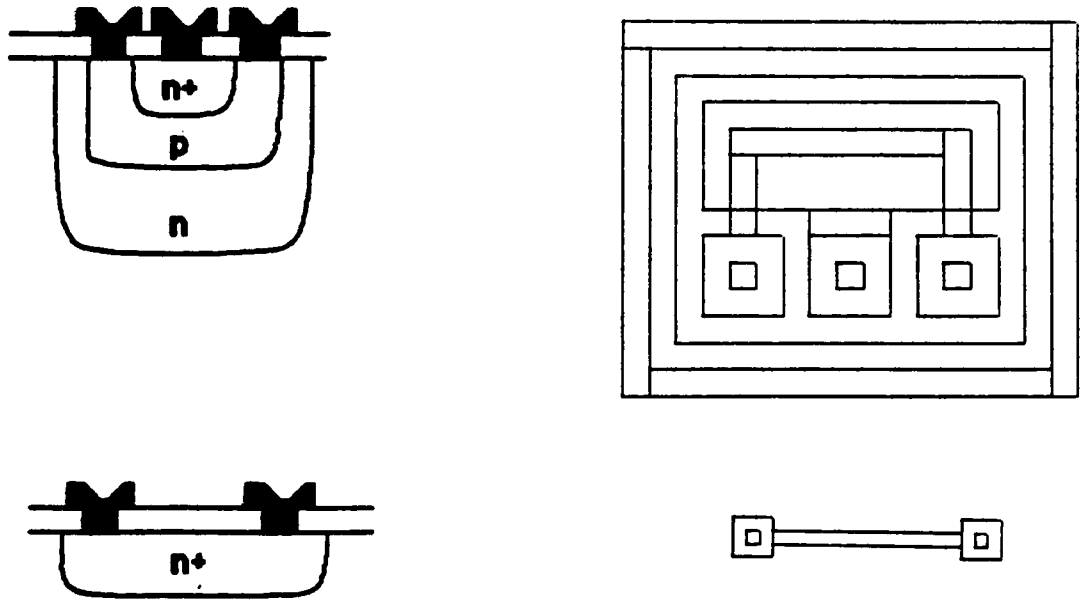


Figure 4.2: Pinch and Emitter resistors

were discounted due to their comparatively small values. A corner is normally only 2/3 of a square, and the clubhead, or area surrounding the contact, has some resistance[8].

The base resistors require a p-type ring around them. This is known as a "guard ring," and it does three things. First, it prevents parasitic NMOS transistors from forming between N-wells. Second, it stifles parasitic lateral bipolar NPN transistors. Third, it provides a better electrical contact to the substrate by providing a lower resistance path. These rings are not required in emitter resistors. When designing a circuit, several contacts should be made to the guard ring to minimize voltage drops within the ring.

Figure 4.1 also shows the top view of a completed base resistor. This resistor is designed from the inside out. The p-type diffusion is laid out according to calculations, and clubheads and contact cuts are drawn it at the resistor ends. The structure is then surrounded with the N-well, and an emitter level "plug" with contact cuts inside is placed inside the N-well with a 10 micron overlap. These emitter plugs prevent Schottky diodes from forming at the N-Well/ aluminum interface and again provide a good low resistance contact. Next, the guard ring is placed around the N-well and a contact cut put into the ring. Note: this is not how the resistor is fabricated (see Chapter 2), merely a method of designing it for fabrication. The emitter resistors are designed with the same method as the base resistors, except

that emitter resistors need no N-well isolation. Pinch resistors, on the other hand, are simply base resistors with an emitter diffusion over the p-region. This effectively reduces the current flow area and increases the resistance. Pinch and emitter resistor layouts are shown in Figure 4.2.

TRANSISTOR DESIGN

The transistor design was simpler than the resistor design since no calculations were required. An NPN vertical transistor cross-section is shown in Figure 4.3. For a vertical transistor layout is easy since each layer is totally inside the next layer. For the 10 micron minimum geometry device in Figure 4.3 the 30 um by 30 um emitter area was first. Surrounding this was a 70 micron by 50 micron base. Contact cut space accounted for the extra 20 microns. Next, the N-well was extended 10 microns beyond the base on three sides and 50 microns on the fourth. Again, the extra extension left room for a contact. In the N-well contact area a 30 um by 30 um plug was placed to avoid Schottky diode problems at the N-Well/aluminum interface. Finally, the contact cuts were put 10 microns inside the contact area for each region, and p-type guard ring was drawn in 10 microns beyond the N-well.

A lateral transistor is slightly different from a vertical transistor. As the name implies, current in a lateral transistor flows parallel to the wafer surface. The

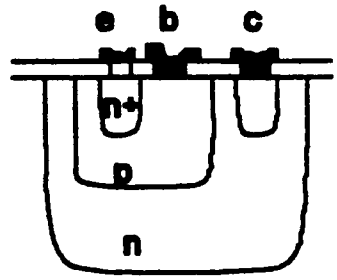


Figure 4.3: NPN vertical transistor cross-section

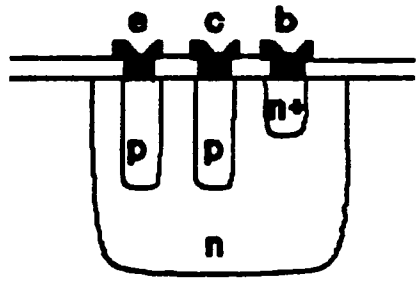


Figure 4.4: Lateral PNP transistor cross-section

emitter and collector are diffused into the wafer adjacent to one another. The transistor base is the region between the two diffused areas. A lateral PNP transistor is shown in Figure 4.4.

Figure 4.5 shows a cross-section of the many different discrete devices. Note that NMOS and PMOS transistors are also shown. These devices were simply available to users who wish to place an MOS structure in a circuit.

To use a standard cell the designer chooses the desired cell from the library. The library specifies the pertinent cell information such as function and physical dimensions. Once the cell is chosen, it is pulled into ICE and positioned in the design. Further connections are added as necessary and the design is saved as a new cell. New cells can be used to make larger designs.

CIRCUITS

Once the simple cells were designed, several were used to form the various section of an operational amplifier. A simplified 741 op-amp schematic was used as the target design; however, due to process limitations the actual op-amp design deviated from the 741 design shown in Figure 4.6[8]. There are four basic sub-circuits to this design: the differential amplifier, the op-amp current source, the high gain stage and the output stage.

The major problem in designing this circuit was the PNP transistors. The RIT N-well process had only produced

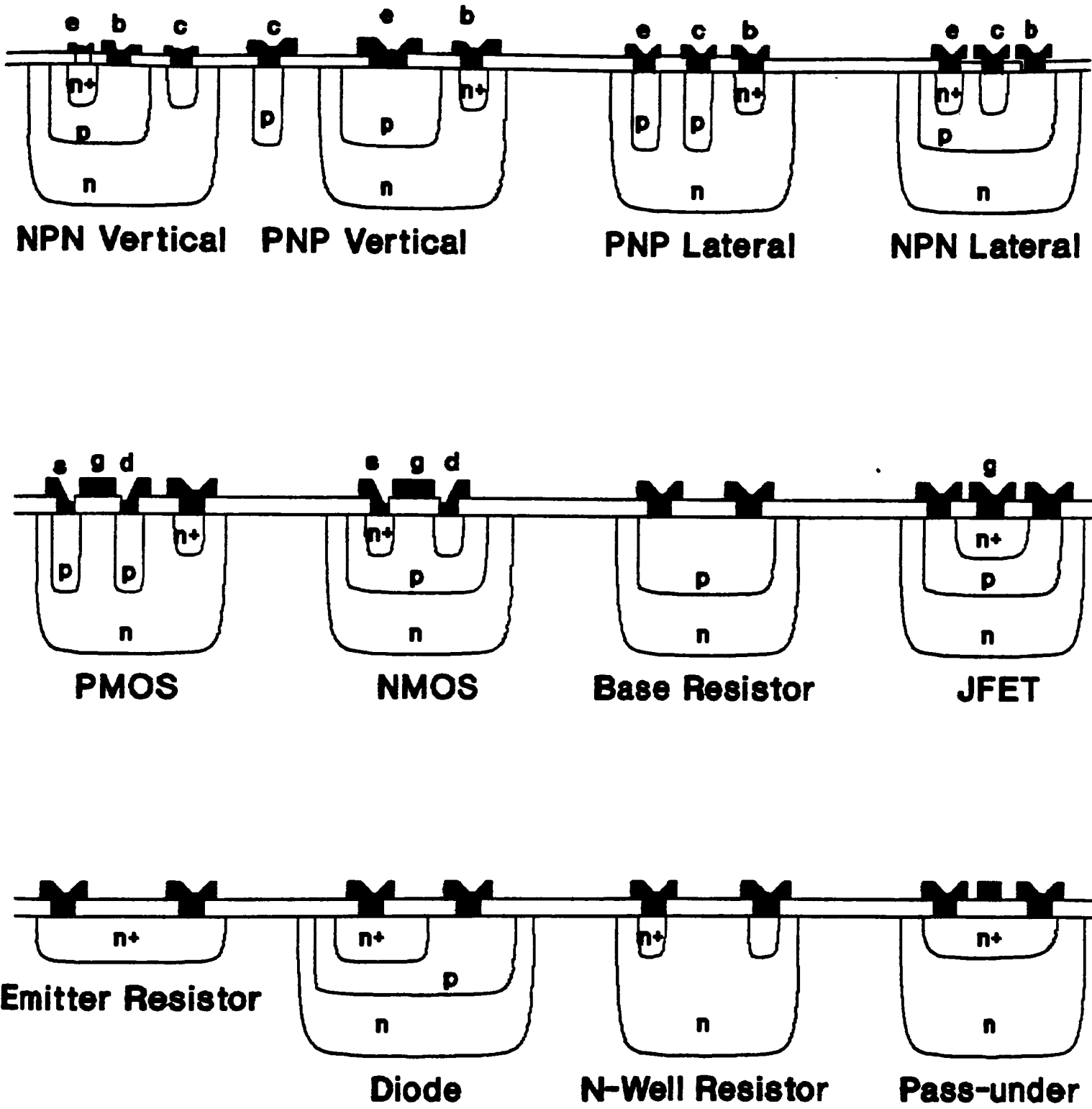


Figure 4.5: Various device cross-sections

substrate PNP transistors, meaning the collector was always connected to the negative rail (-5 volts). Without the non-isolated PNP transistors, the PNP current sourcing and level shifting between the gain and output stage were not possible. The redesigned op-amp is shown in Figure 4.7. It uses two cascaded resistor pull-up differential amplifiers for gain, a current mirror current source, levelshifting resistors and an AB output stage.

CURRENT MIRROR

The current mirror was designed first, and the schematic is shown in Figure 4.8. Transistor Q1 was used as a diode so V_{ce} is approximately .7 volts. The current flowing through Q1 is determined by R1 in equation 4.1.

Eq. 4.1 $$I_{ref} = (V_{cc} - (V_{ee} + .7)) / R1$$

where V_{cc} = positive supply rail (5 volts)
V_{ee} = negative supply rail (-5 volts)
I_{ref} = resultant current flow

To have a reference current of 200 microamps R1 is 46.5 kohms. This reference current was chosen since it is well below the 1 milliamp high level injection limit. Since the B-E junctions of Q1 and Q2 are in parallel, they have identical current flows (i.e., I_{Q2} mirrors I_{Q1}). Q1 can

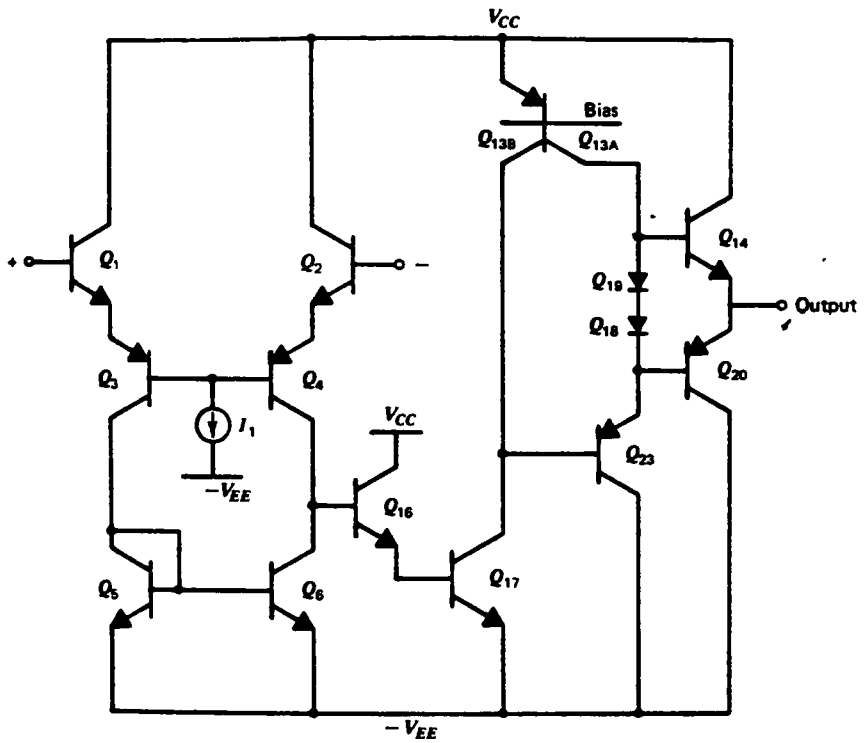


Figure 4.6: Simplified 741 operational amplifier

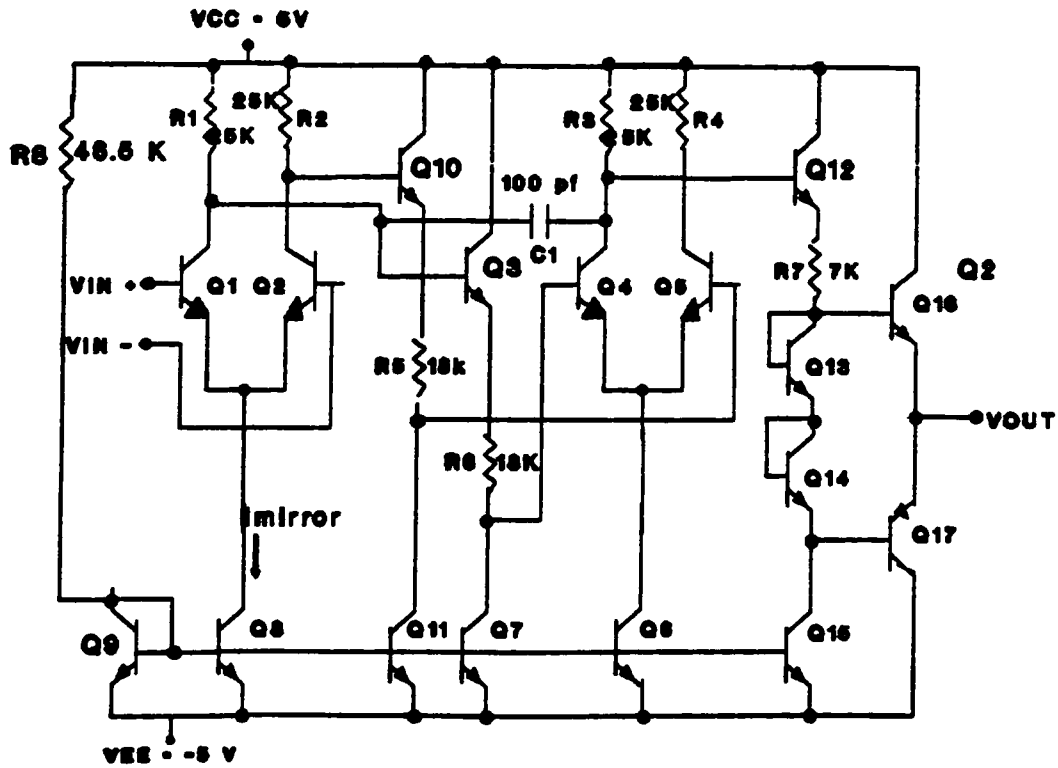


Figure 4.7: Redesigned operational amplifier

mirror several transistor currents before it becomes too loaded to be a valid approximation[8]. This current mirror was used as the current source for the differential amplifier.

DIFFERENTIAL AMPLIFIER

The differential amplifier is used to amplify a small change between its input voltage levels. The schematic for the differential amplifier is shown in Figure 4.9. If the voltage source Vin is connected as shown, it forward biases Q3 and turns off Q4. When Q4 is off, the output voltage is pulled up to the 5 volt supply rail. If the Vin polarity is switched, then Q4 is on and Q3 is off. When Q4 is on, it sinks current through R_2. The output voltage will be determined by Equation 4.2.

Eq. 4.2 $$V_{out} = Vcc - (I_{Q4} \times R_2)$$

where
V_{out} = Output voltage
V_{cc} = Positive supply rail (5 volts)
I_{Q4} = Mirrored current (I_{ref})
R_2 = Pull-up resistor

The voltage will drop only as far as the Q4 base voltage; otherwise the C-B junction will become forward biased. The current mirror current defines IQ4 since it sinks current independent of the differential amplifier. If both transistors are on with the same input voltage then Iref will

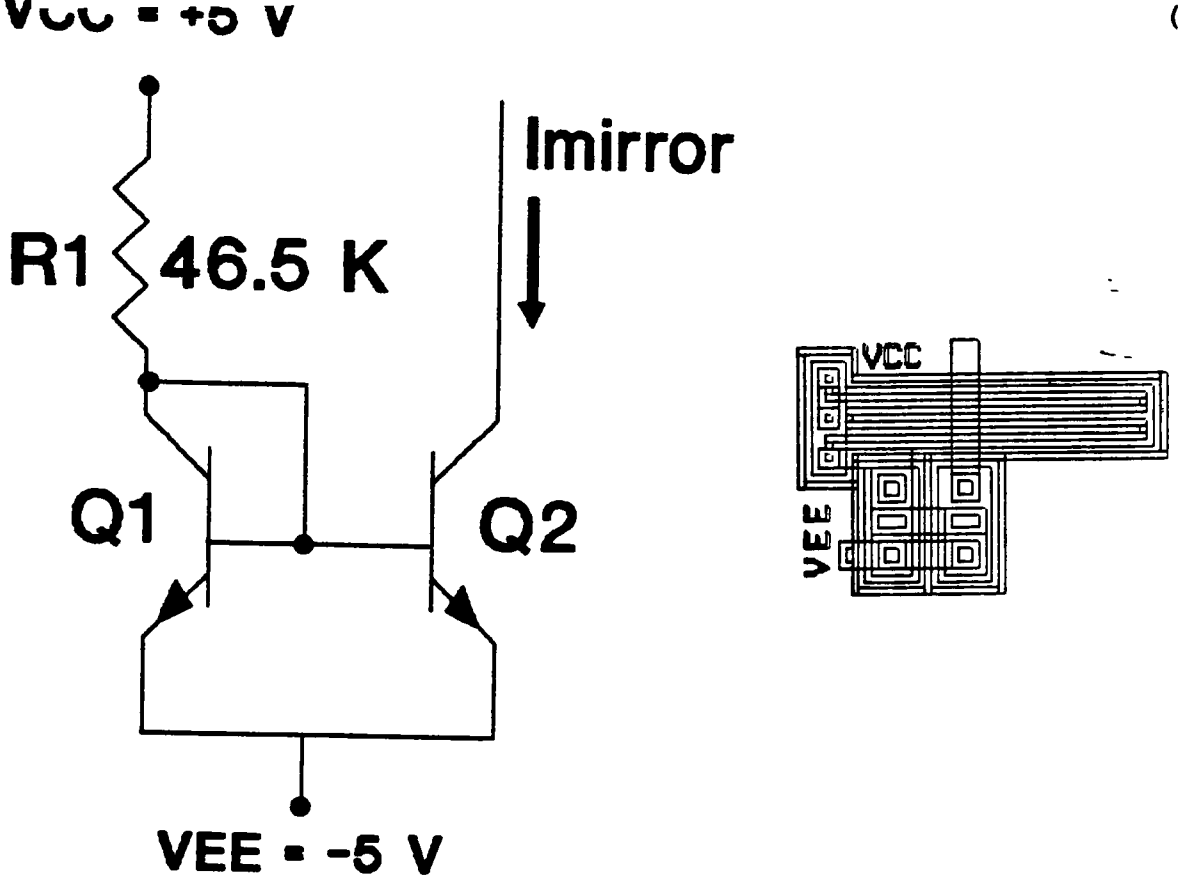


Figure 4.8: Current mirror schematic and layout

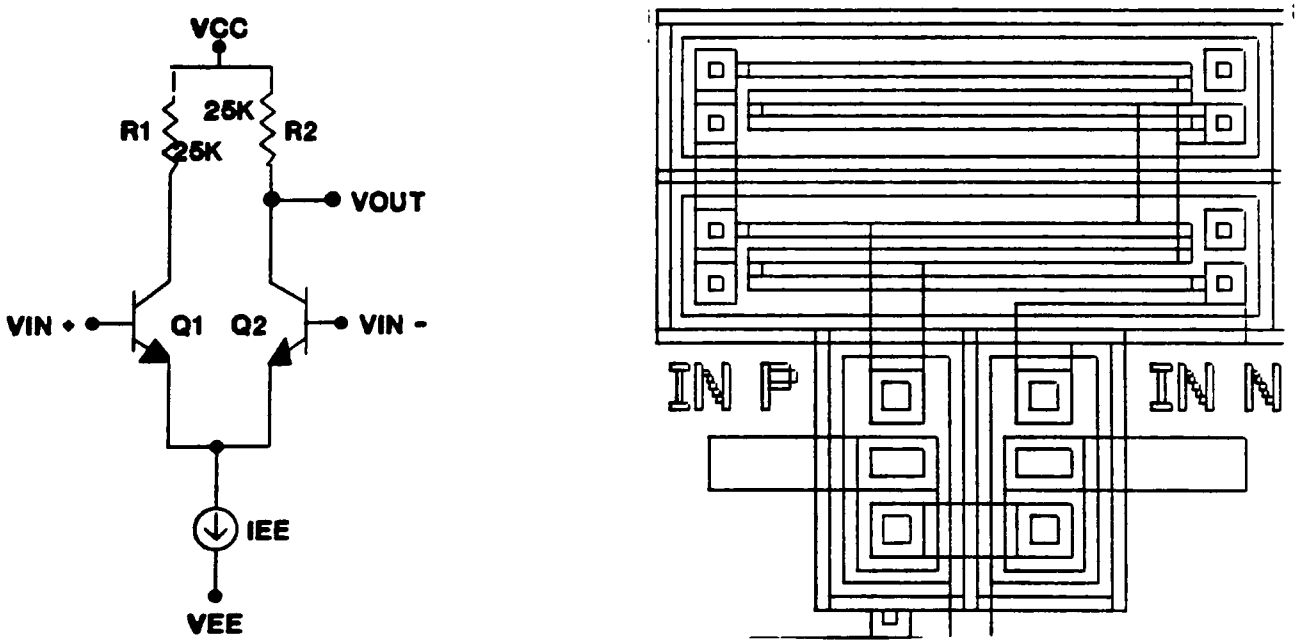


Figure 4.9: Differential Amplifier schematic and layout

split equally between Q4 and Q3. The output voltage will drop 5 volts if Q4 is on, Q3 is off, R4 is 25 kohms and Iref is 200 microamps.

The key to the differential amplifier is the gain, A_v, or how quickly the output changes with a small input change[8]. Equation 4.3 shows this in equation form.

Eq. 4.3 $$A_v = \Delta V_{out} / \Delta V_{in}$$

When modelled with SPICE, the differential amplifier in figure 4.9 produced a gain of 60. This gain is known as the differential mode gain because it examines the gain as two different inputs are applied. The higher the gain the better. Another type of gain, the common mode, was not examined and was assumed to be close to zero, which is desired.

THE LEVELSHIFTER

The next circuit section designed was the levelshifter. The levelshifter allows the voltage output to be lowered to maximize symmetric output voltage swing[8]. For example, if the desired output swing is $\pm$ 2.5 volts and the actual output voltage swing is between 5 volts and zero volts then the five volt range must be lowered by 2.5 volts. The levelshifter schematic is shown in Figure 4.10.

The input voltage is 5 volts. Approximately .7 volts is

dropped across the B-E junction of Q1, and 1.8 volts is dropped across R1. R1 was selected according to the current flow in Q1, which was defined by a 200 microamp current mirror. The output voltage can be only shifted downward with this method. This circuit also act as a buffer between the previous and subsequent stages.

OUTPUT STAGE

The final circuit designed for the operational amplifier was the AB output stage shown in Figure 4.11. The AB output stage has two functions: it buffers the previous circuitry from the next stage and provides symmetric output swing free of diode turn-on effects. Key to this type of stage are the transistors Q1 through Q4. The transistors Q1 and Q2 are connected as diodes (collector and base shorted), and since these junctions are in parallel with the B-E junctions of Q3 and Q4 the voltage drops across the two sets of junctions are identical (approximately 1.4 volts). It was assumed that all junction built-in voltages were matched and that Q1 and Q2 were always on due to the current source.

As a positive input is applied to the stage the voltage drop across the Q1 B-E junction increases slightly, and the voltage across the Q4 B-E junction decreases slightly to maintain the proper voltage drop. This effectively shuts of Q4. When a negative input is applied, Q3 shuts off with the same reasoning. The disadvantage of this stage is a 1.4 volt shift in the output curve. This can be offset by placing a

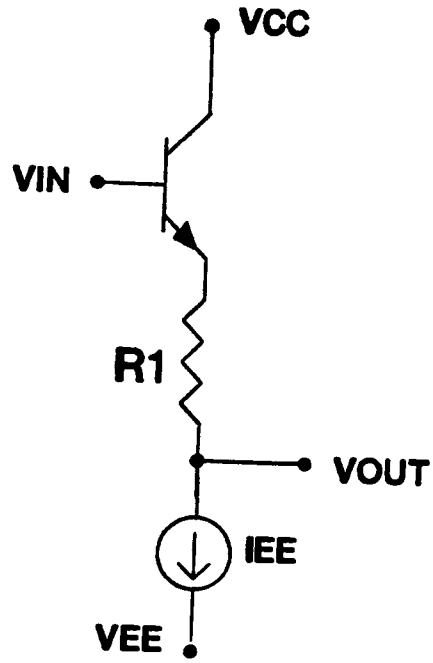


Figure 4.10: Levelshifter schematic

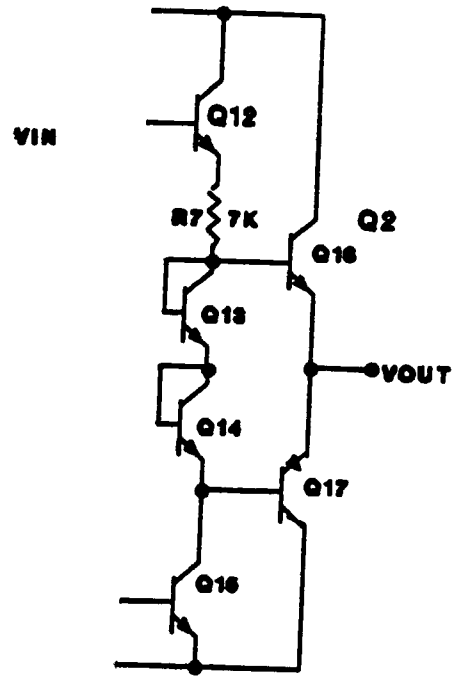


Figure 4.11: Output stage schematic

levelshifting resistor in series with the Q5 B-E junction. Transistor Q5 also provides the buffering action, since current will not flow backward through the transistor but will be sunk by Q4 to the negative supply.

DARLINGTON CIRCUIT

The Darlington circuit, also known as the common collector-common collector circuit, is basically two transistors cascaded together, but acting as one. The current flowing out of Q1 flows into the base of Q2. As a result, the Q1 base current is amplified twice: once by each transitor. This connection can essentially square the gain of one transistor, assuming the transistors are matched. Figure 4.12 shows the schematic and layout for a Darlington circuit.

IIL NOR/AND GATE

Although the process is for analog circuit fabrication, an IIL circuit, a digital technology, was included for two reasons. First, it is desirable to have a process that is multi-functional. Second, an IIL circuit uses two bipolar devices: a lateral PNP transistor and a vertical NPN transistor[5].

The IIL circuit uses the PNP device to turn on the NPN device. A cross-section is shown in Figure 4.13. As current is injected into the p-type region, the pn junction becomes forward biased and places the lateral device in active mode

operation. The PNP emitter is also the NPN base, and the emitter current from the PNP transistor flows into the NPN and turns it on as well. When the NPN transistor is on, the emitter voltage is pulled low; otherwise it is high. The result is a digital switching action. These circuits can be cascaded together to form all types of digital gates. The IIL circuit schematic and layout are shown in Figure 4.14.

OPERATIONAL AMPLIFIER

The four circuits discussed were designed together to form an operational amplifier, as shown in Figure 4.7. There are two differential amplifiers in the circuit to improve the overall gain. Cascading two stages together squares the gain of one. In this case, the total gain is approximately 60 squared, or 3600. A high gain is necessary for an effective op-amp.

As mentioned, no active loads were used since the available lateral PNP transistors did not work properly. Active loads are normally used in integrated circuits because they save chip real estate. However, resistors and levelshifters were used in place of the active loads. The major drawbacks are increased area and higher power consumption, but resistors do allow a larger output voltage swing.

SPICE simulations were used extensively in the op-amp design, and they are located in appendix 4.1. The AC simulation raised the question of frequency compensation. If

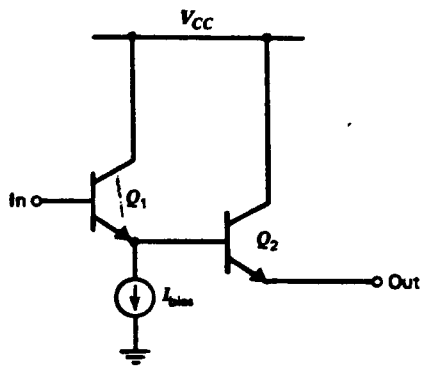


Figure 4.12: Darlington schematic

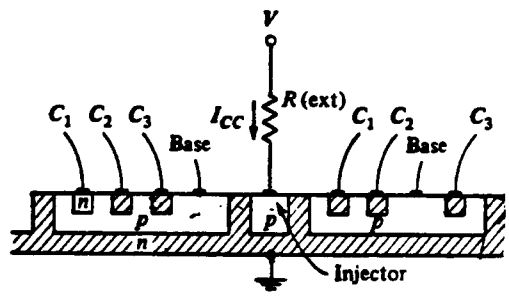


Figure 4.13: IIL cross-section

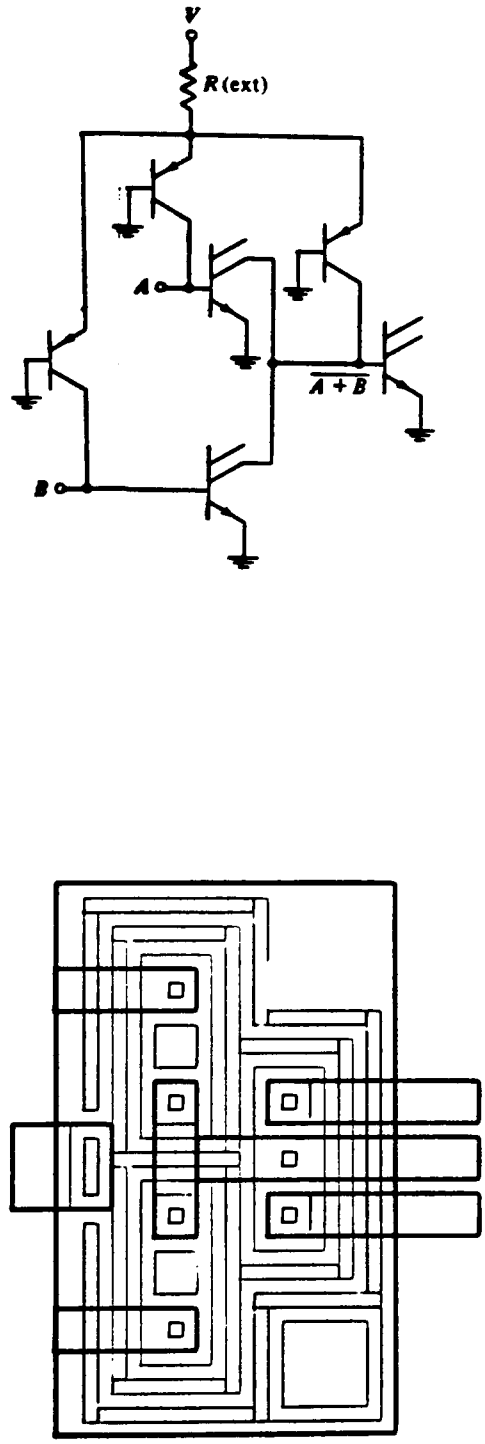


Figure 4.14: IIL NOR/AND gate schematic and layout

the phase margin, or frequency shift, between the input and output signals reach a difference of 180 degrees before the circuit gain drops to one, then the circuit will oscillate if used near this operating region. In this case the circuit must be compensated for this frequency shift[8]. The easiest method of compensation is to add a pole to the transfer function that would pull the gain to one (unity gain point) before the circuit oscillates. This was done for the op-amp and is shown below in Equation 4.4.

Eq. 4.4 $\quad abs(p_d/(2 \times pi)) = 1/a_o \times abs(p_1/(2 \times pi))$

where p_d = the desired dominant frequency
p_1 = the present dominant pole
a_o = low frequency gain (A_v)

For p_1 = 20 kilohertz (kHz), a_o = 3600, and pi =3.142 then p_d is 16.67 hertz (Hz). This new dominant pole is equal to:

Eq. 4.5 $\quad p_d = 1 / (2RC)$

where C = the desired compensation capacitance
R = AC resistance in parallel with C

This capacitor was placed between the collector of Q1 and ground. It was assumed that RC1 was R since RC1 is in parallel with the C-B junction of Q1 and Q7, which are taken

as infinite resistance paths. C was found to be .3 microfarad and was too big to be fabricated on chip. To avoid, this the Miller capacitance was used, and a conversion calculation was performed using equation 4.5[8].

Eq. 4.5 $$C_1 = C_2 (1 - V_2/V_1)$$

where C_1 = the old compensation capacitance

C_2 = the new compensation capacitance

V_2/V_1 = the low frequency gain

The new compensation capacitance was found to be 250 picofarads (pf).

According to the op-amp SPICE simulations, a capacitance of 31 pf was sufficient to compensate the op-amp using Miller capacitance. The capacitor was placed between the collectors of Q1 and Q4. The new cutoff frequency, or frequency at the unity gain point, was 780 kHz. The 100 pf capacitor was used since it left room for error, was still smaller than the predicted value and conserved chip area. The capacitor area calculation is shown in Equation 4.6.

Eq. 4.6 $$AREA = (C)(T_{ox}) / (E_{si}E_o)$$

where C = Compensation capacitance F

T_{ox} = Dielectric thickness (SiO2) cm

E_{si} = Permittivity of silicon

E_o = Permittivity of free space

$= 8.85 \times 10^{-14}$ F/cm^2

The capacitor area was calculated to be roughly 300 square microns.

Once the circuits were designed schematically they were laid out using ICE and the RIT N-Well Bipolar design rules. Each circuit was separately placed on a testchip design for fault isolation should the op-amp not operate after fabrication. All layouts are located in appendix 4.1, as part of the standard cell library.

CHAPTER FIVE: RESULTS

Three fabrication runs were completed and tested. The The fabrication process was demonstrated in Chapter 3, and an HP4145 Semiconductor parameter analyzer was used to test most of the circuits listed in Chapter 4. As the testing results from each fabrication run were examined, process changes were made to improve the results.

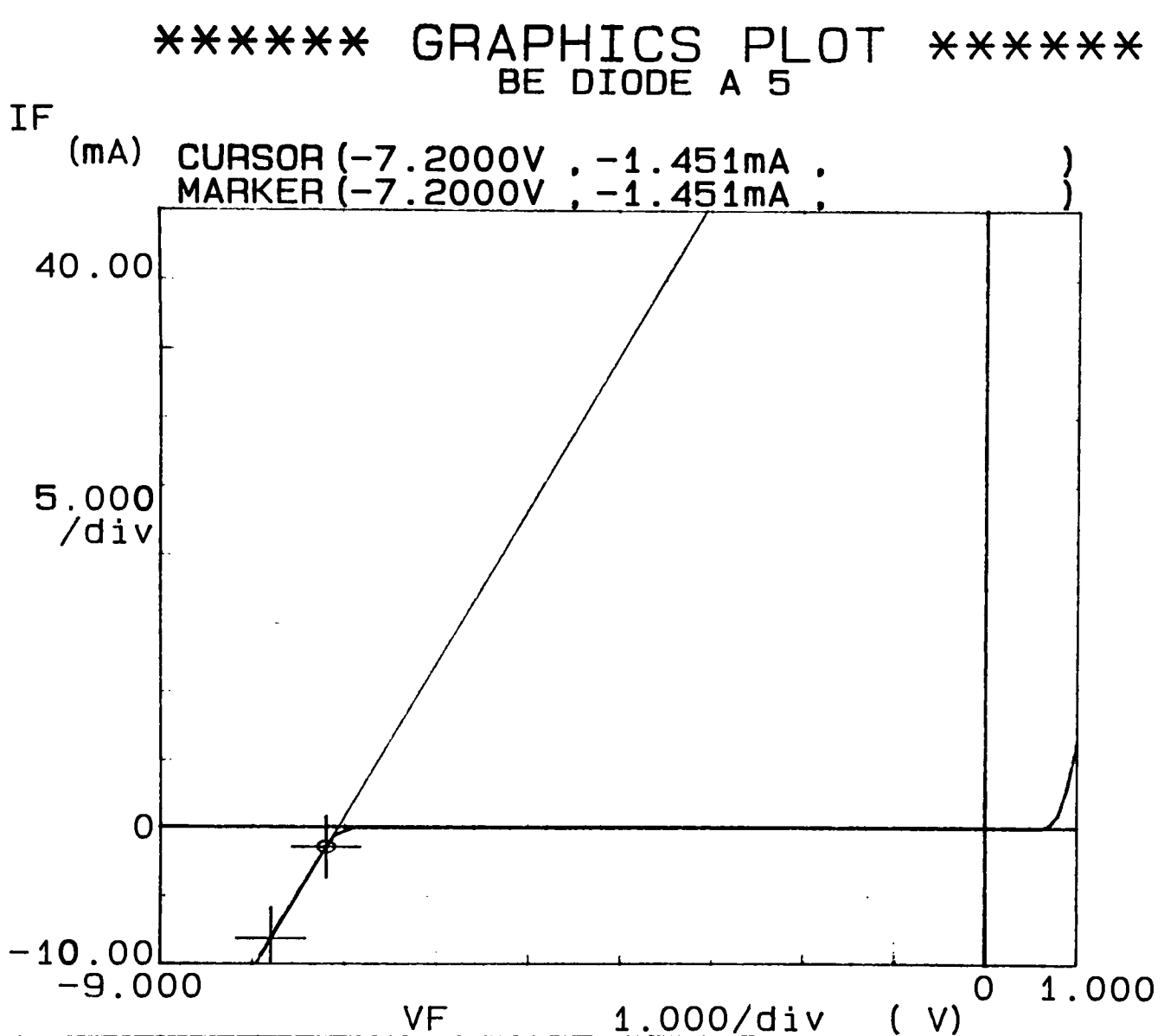
FIRST RUN

The first processing run (3/90) merged existing non-isolated bipolar and deep N-Well processes. This method was attempted first because the use of solid sources in the process was not very predictable, but was repeatable, and the author of this text did not yet fully understand the device physics required for process development. The first testchip included NPN, PNP, and MOS transistors, split-cross and contact resistance test structures, resistors on all diffusion levels, an IIL circuit, a Wilson current source and a Darlington circuit.

Two wafers from the first lot were processed through emitter pre-deposition and tested for transistor action. After SUPREM simulations, consultation with Dr. I. Renan Turkman, device physics calculations, and no observable transistor action it was concluded that the base Gummel number of approximately 10^{14} atoms/cm^2 was too high for transistor action to occur. To correct the situation an

extended emitter drive-in at a lower temperature than planned trapped boron dopant in newly formed SiO_2 but did not push the emitter very far into the wafer. The finished NPN transistors still did not work, but the forward bias and breakdown characteristics for the base-emitter pn junctions operated quite well, as shown in Figure 5.1a. Several substrate PNP transistors produced a gain of 20, but only after the base-collector junction was reversed biased to -6 volts. These factors, combined with revised SUPREM III runs, indicated that the base doping level was too high and the physical base width was too wide.

A third wafer that had been held back prior to emitter predeposition was reworked with appropriate process changes, completed and tested. The emitter predeposition was done at $975^{o}C$ with a 10 minute soak time, and the subsequent diffusion was 15 minutes in wet O_2 at $1100^{o}C$. The NPN transistors produced gains of 40 - 50 at base currents of 1 uA to 10 uA, as shown in Figure 5.2. The collector resistances were on the order of 1 - 5 kohms, which was expected since there was no buried layer in the process. The output resistance was high at greater than 30 kohms, and this was desired for good analog circuit design. The output resistance was probably higher, but surface leakage significantly affected the transistor characteristics. The split-cross structures produced high sheet resistances, but this was expected from the solid diffusion sources. Contact resistances for the base and emitter regions were in the



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	11.2E-03	89.3E+00	-7.07E+00	79.2E-03
LINE2				

Figure 5.1: Base-emitter junction characteristic, 1st run

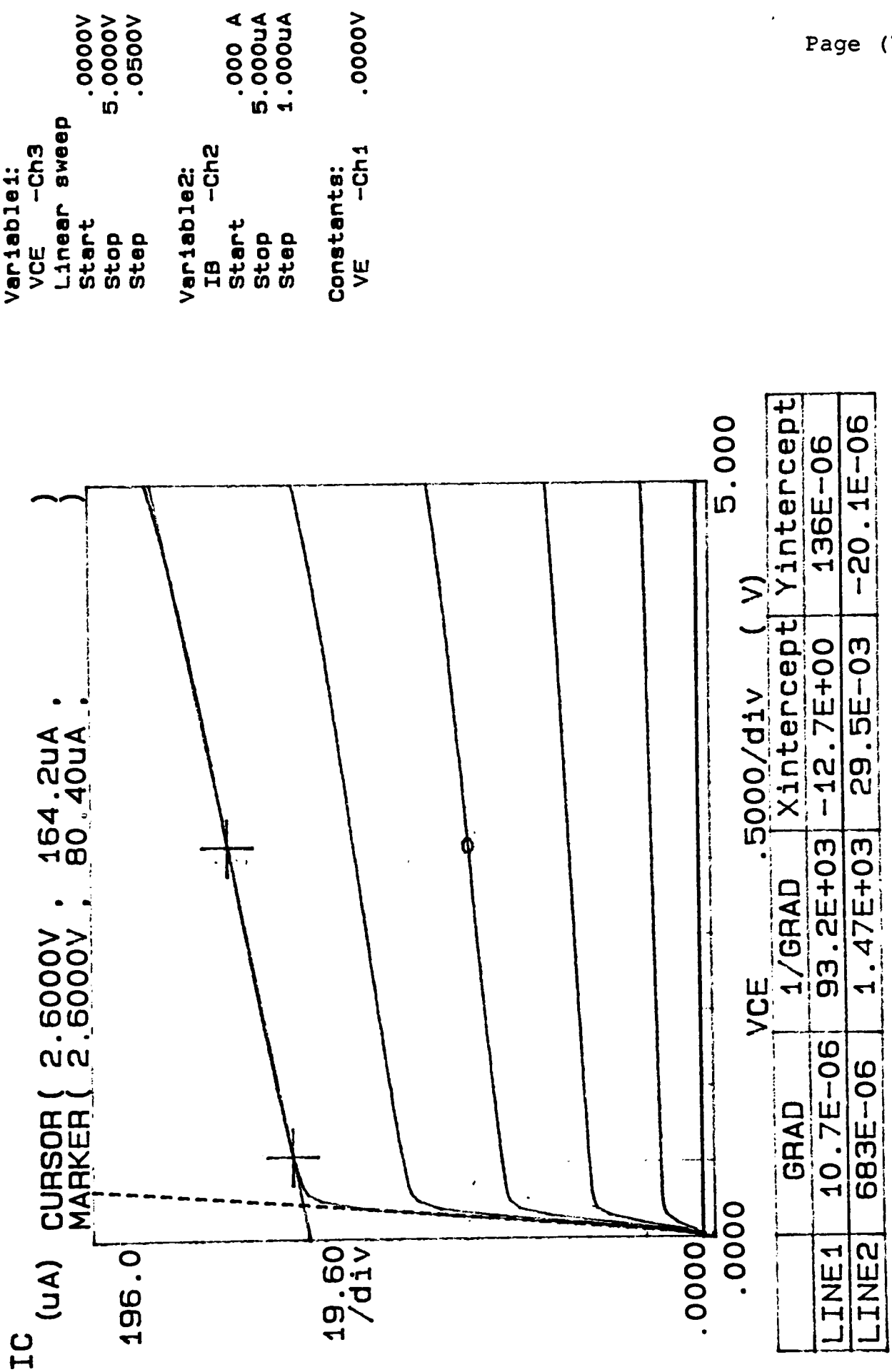


Figure 5.2: NPN characteristic, reworked 1st run

range of 2 ohms, which was very good. Extensive testing was not performed on this run since the process required basic enhancements. Also, the I_c versus V_{be} plot was examined, and at once testing was stopped since it confirmed that the process needed basic revisions. The testing results are are summarized in Table 5.1 below.

Parameter	Calculated	Measured
V_{bi}	1.035 volts	on at .874 V
$BETA_{npn}$	26	40 - 50
BV_{ceo}	7.6 volts	8 - 10 V
V_a	- 326 volts	-25 V (best)
R_c	-----	1.47 kohms (best)
R_o	6.1 Mohms	2 Mohms (best)

Table 5.1: Testing results from the revised 1st run

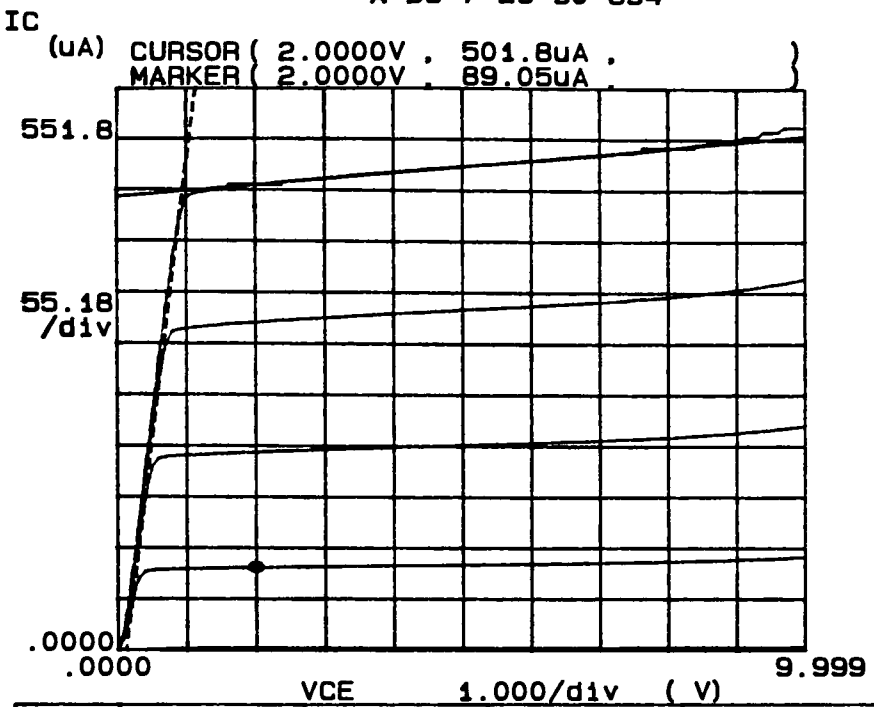
SECOND RUN

The major goals for the second processing run were to characterize the discrete bipolar transistors and produce simple working circuits. Overall, the second run produced better results: the NPN and PNP Betas increased, the Early voltage was good, the breakdown voltage was satisfactory and the collector resistance was predictable.

The second process was designed with a better knowledge of what affected the operating parameters, and as a result a

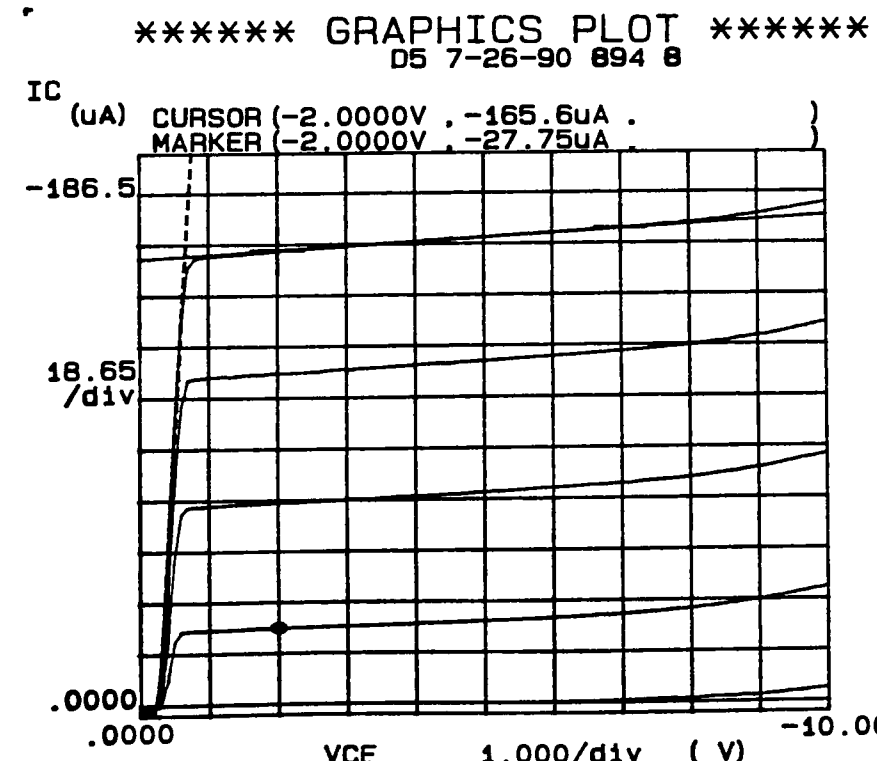
better process was developed. SUPREM III was used to simulate a process that would produce target doping values for each transistor region. The target values were appropriate for a "typical" transistor: emitter doping equal to 1×10^{20} atoms/cm^3, a base doping of 8×10^{16} A/cm^3 and a collector doping of 8×10^{15} A/cm^3 [7]. A lower substrate doping level was also chosen to allow the lowered collector doping level, and in turn a lower base doping level. The N-Well drive-in was adjusted to reflect this change. A basewidth between 1 and 1.5 microns was also targeted. Finally, the device parameters were calculated from SUPREM III output files with the vertical NPN and substrate PNP transistors primarily considered (see Chapter 2). Once acceptable theoretical values were obtained, processing was started.

The test results for the vertical transistors were very good. A sample NPN transistor characteristic is shown in Figure 5.3. The average Beta value was approximately 130, while the Early voltage was -75 volts. The collector-emitter breakdown voltage, BVceo, was also good at 16 - 18 volts because it exceeded the region of operation for circuit design. The supply voltages were limited to $\pm$ 5 volts. The collector resistance was an average of 2 kohms, and this was again expected. The vertical PNP transistors also performed much better than those from the previous run. The Beta values approached 40 and the Early voltage was generally much



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	6.75E-06	148E+03	-72.3E+00	488E-06
LINE2	600E-06	1.67E+03	122E-03	-73.1E-06

Figure 5.3: NPN vertical transistor family of curves, 2nd run



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	1.53E-06	653E+03	106E+00	-162E-06
LINE2	421E-06	2.38E+03	-271E-03	114E-06

Figure 5.4: PNP vertical family of curves, 2nd run

higher than 100 volts. The breakdown voltage was consistently higher than 30 volts. A sample family of curves for the device is shown in figure 5.5.

The lateral transistors did not fare as well as the vertical devices. The PNP devices had a Beta of less than one, and as a result testing ceased on the device. The NPN devices had Betas of approximately one, and again testing was not pursued for the device. After further research it was concluded that surface effects and wide basewidths (greater than 1.5 microns) were the major culprits in the poor device operation. Several transistors for each transistor type were tested to explore the process consistency, and the results are shown in Table 5.2. The sheet and contact resistances were found using resistor results and Equation 5.1. By using resistors of two different lengths, Equation 5.1 becomes two equations with two unknowns.

Eq. 5.1 $R = R_S \times (\text{No. squares in resistor}) + 2R_C$

where R = Resistor value (ohms)

R_S = Sheet resistance (ohms/square)

R_C = Contact resistance (ohms)

The resultant emitter level sheet resistance was approximately seven ohms per square, and the resultant base level sheet resistance was close to 225 ohms per square. The contact resistances ranged between 5 and 10 ohms.

Type	BETA	BV (V)	V_a (V)	R_c (ohms)
NPN vert.	115.5	19	-54.2	1.73 k
	131.6	19	-77.4	1.78 k
	52.9	18	-156	2.34 k
	120.5	17	-66.8	1.65 k
	5.5	22	-52.0	7.25 k
	116	17	-65.6	1.81 k
	100.8	17	-59.0	1.89 k
	103.8	17	-57.3	1.97 k
	1.50	>20	-18.6	8.20 k
	3.30	>20	-84.0	21.9 k
PNP sub.	6.98	>30	9.96	13.3 k
	40.07	>30	13.2	2.73 k
	2.5	>30	3.97	9.57 k
	18.67	>30	23.8	5.00 k
	51.24	>30	99.7	2.07 k
	44.18	>30	146	2.28 k
	45.07	>30	161	1.96 k
	40.86	>30	93.6	2.33 k
	40.15	>30	41.1	3.18 k
	31.3	>30	69.9	2.64 k
	43.7	>30	35.9	2.36 k
PNP lat.	.269	>50	28.0	89.9 k
	.283	>50	34.6	27.5 k
	.255	>50	36.8	27.8 k
NPN lat.	.985	>50	-19.2	-----
	.973	>50	-7.88	-----
	1.01	>50	-11.3	-----

Table 5.2: Transistor results, 2nd run

The specific resistor values varied somewhat, but appeared to be within 15 percent of the average value. Only the base and emitter level diffusions produced linear resistors. The base resistors were more extensively tested and the results are shown in Table 5.3. The emitter resistors were spot tested only. The N-well resistors had two problems. First, there was a Schottky diode at the well/metal contact due to a light N-Well doping[7]. Second, as the resistor voltage drop increased, the N-well channel was pinched by depletion region extension. The effect was an increased resistance.

There were four main circuits fabricated on the second chip: an IIL nor/and gate, a Darlington circuit, a Wilson current source and a biased transistor circuit. Processing problems hampered most of these circuits. The lateral pnp failure had prevented the IIL circuit from working since the lateral pnp is a critical device in IIL operation. The non-linearities in the N-well resistors affected the Wilson current source and the biased transistor circuit since both utilized the N-well resistors as DC biasing elements. The Darlington circuit worked very well. To avoid high level injection effects base currents in the 1-5 nanoamp range were applied to the Q2 base. These low base currents were extremely susceptible to noise, as shown in figure 5.4, but the family of curves is distinguishible. The Beta for this circuit should be the gain of one transistor squared, but the noisy plot made it difficult to obtain accurate information.

Sample	BR1	BR2	BR3	BR4	BR5
1	4.5 k	6.19 k	9.49 k	15.6 k	22.4 k
2	3.53 k	5.85 k	9.29 k	15.9 k	22.3 k
3	3.55 k	5.94 k	9.39 k	15.8 k	22.3 k
4	3.38 k	5.99 k	9.37 k	15.7 k	22.4 k
5	3.47 k	5.94 k	9.26 k	15.9 k	22.4 k
6	3.51 k	5.95 k	9.23 k	15.7 k	22.2 k
7	------	7.43 k	9.31 k	17.2 k	------
8	4.35 k	11.6 k	11.5 k	18.4 k	22.4 k
9	3.67 k	6.25 k	9.65 k	15.9 k	27.0 k
10	------	5.76 k	13.1 k	15.9 k	27.1 k
Mean	3.75 k	6.69 k	9.96 k	16.2 k	23.4 k
Std. Dev.	.429 k	1.79 k	1.30 k	.896 k	2.06 k

Note: There was a one hour break in testing between samples six and seven. Calculations reflect measurable values.

Table 5.3: Base resistor results - 2nd Run

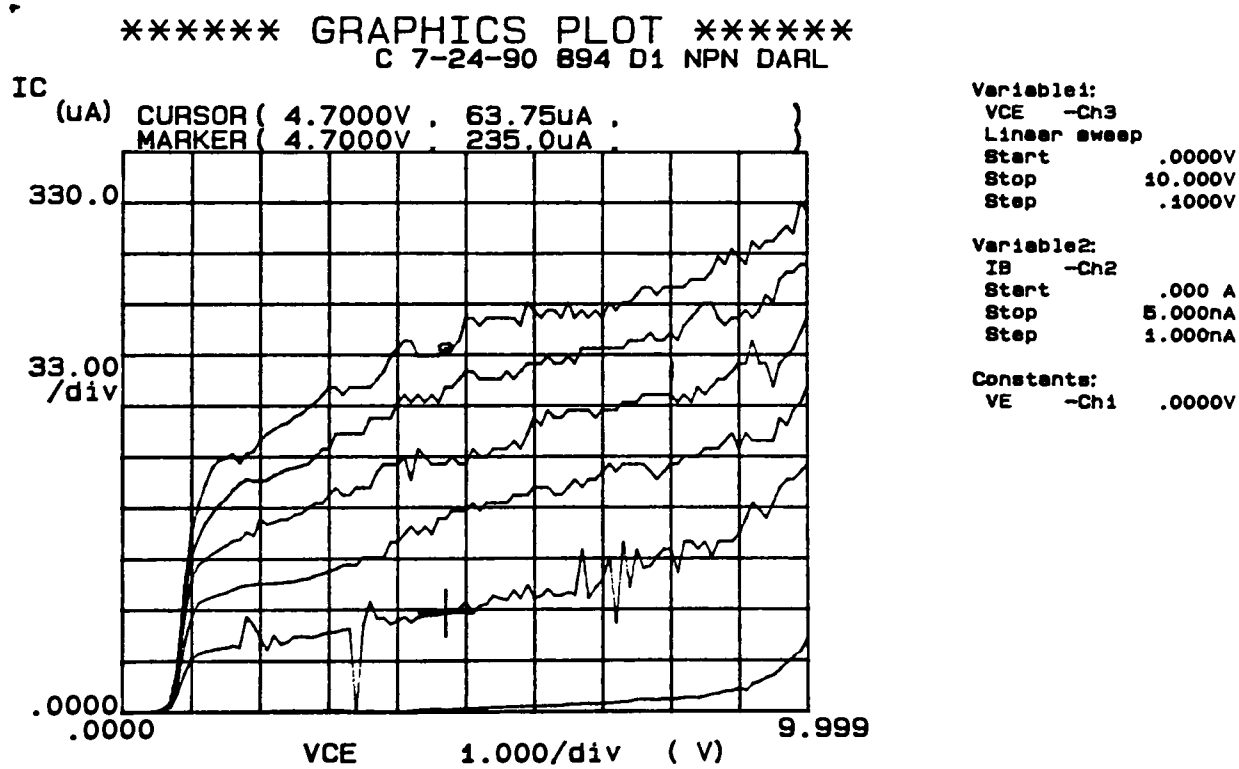


Figure 5.5: NPN Darlington output curve

The vertical transistors produced results that were in line with device physics calculations, but the lateral transistors did not. Surface damage seemed one of the probable causes for this so a gettering process was designed for the third processing run in hopes of eliminating surface damage and contaminants[1]. The sheet resistance values were fairly uniform across the wafer and from wafer to wafer, as indicated by resistor testing. These values were used to design resistors for the third run. The process produced its first working circuit, but the percentage of consistently working devices raised concern for the design of larger circuits.

THE THIRD RUN

The third and final fabrication run had two purposes. First, is was used to verify that the process worked. Second, it was used to fabricate larger circuits and move the process into the "manufacturing" phase. A gettering process was introduced to help solve the lateral transistor problems. Several devices and circuits were successfully tested including a differential amplifiers, current mirrors, and an operational amplifier.

The first devices tested were the vertical NPN transistors. The beta values changed with the level of collector current, which was unexpected. When the collector current was below 100 uA, beta was approximately 100. Above

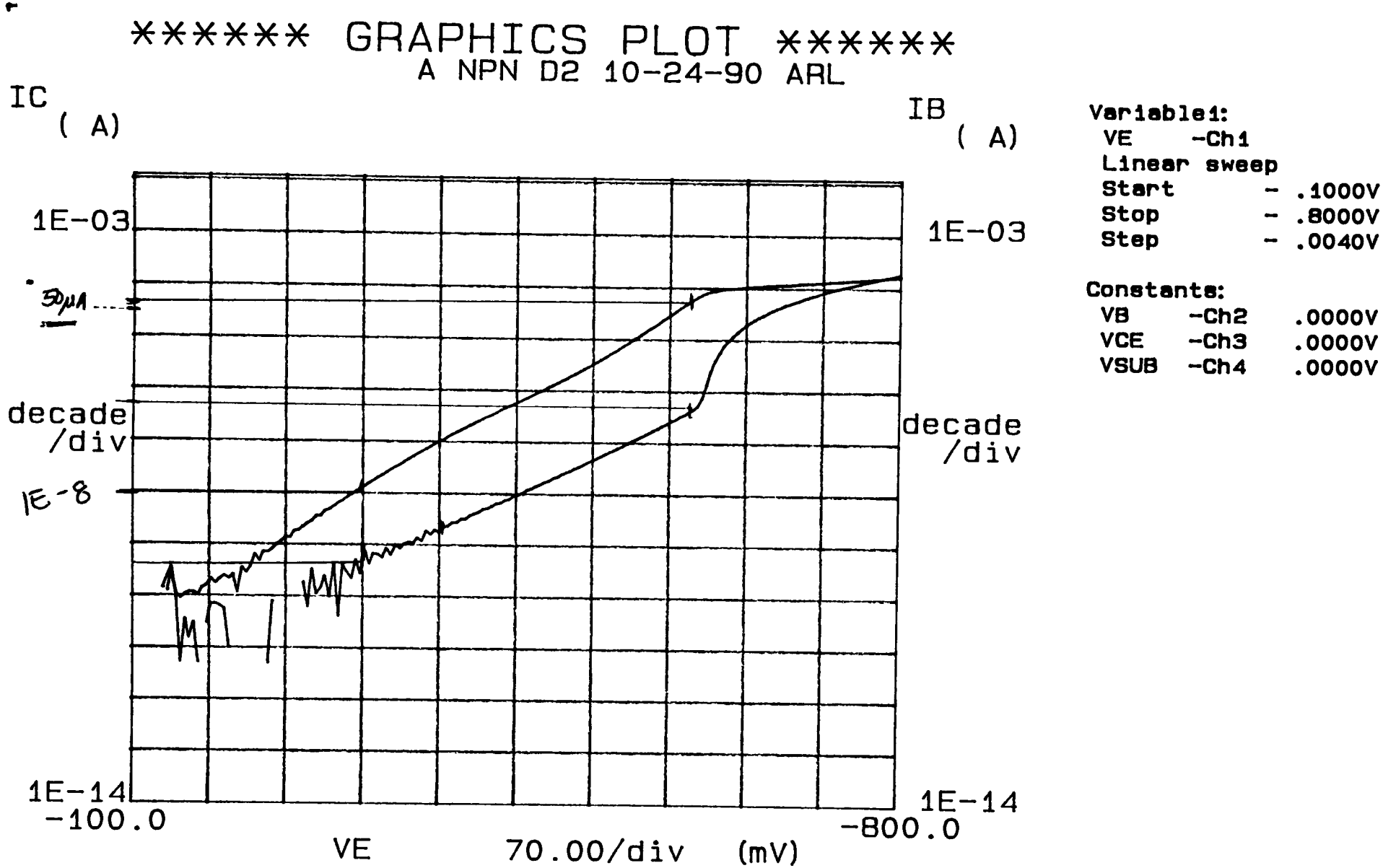


Figure 5.6: NPN vertical Ic vs. Vbe curve showing roll-off

100 uA, beta increased to over 200. A plot of I_c and I_b versus V_{be} shows this effect in figure 5.6. When the high level injection roll-off point was located it showed that the threshold limit was approximately 100 uA (see chapter 6 for more discussion). This was much lower than the previous fabrication run by almost a factor of 10. However, it was concluded that the C-B junction became slightly forward biased for the I_c versus V_{be} testing which would indicate a lower roll-off point. The breakdown voltage also decreased from 15 volts to 13 volts. Both of these factors indicated that the base doping was too light. However, the consistency of operation had increased as shown in table 5.4.

Beta	BVceo (v)	Va (v)	Rc (kohms)	Ic (uA)
85.3	13.0	-109.0	21.3	40
76.7	13.0	-39.2	31.3	40
71.7	13.0	-12.9	8.5	50
93.0	12.5	-92.9	27.3	40
101.2	13.0	-91.4	26.4	40
102.1	13.0	-102.0	5.67	40
95.4	14.0	-25.0	10.3	40
77.3	13.5	-21.5	14.2	35
45.6	15.0	-138.0	12.0	25
84.9	14.0	-96.3	15.8	40
x = 83.3	13.4	-72.7	17.3	39.0
o = 16.85	.74	44.0	8.80	6.15

Table 5.4: NPN Transistor results

The PNP vertical transistors produced similar results, as shown in table 5.5, but the beta values were slightly lower than expected. Again this pointed to a light base doping. The gettering process did not solve the problems with the lateral devices since the beta values were unchanged.

Beta	BVceo (v)	Va (v)	Rc (kohms)	Ic (uA)
11.62	+20	infin.	8.20	-50
10.43	+20	infin.	6.43	-50
12.48	+20	infin.	5.16	-50
11.31	+20	infin.	5.02	-50
11.84	+20	infin.	6.38	-50

Table 5.5: small vertical PNP transistor results

One item that was noticed was the failure of a large geometry vertical PNP transistor. The emitter area was approximately three times that of the minimum geometry device. It was concluded that this transistor failed because of the lateral base resistance. The current travelling from the base contact to the junction caused the biasing voltage to drop, and the B-E junction was not forward biased as a result. The result was a nonfunctioning transistor.

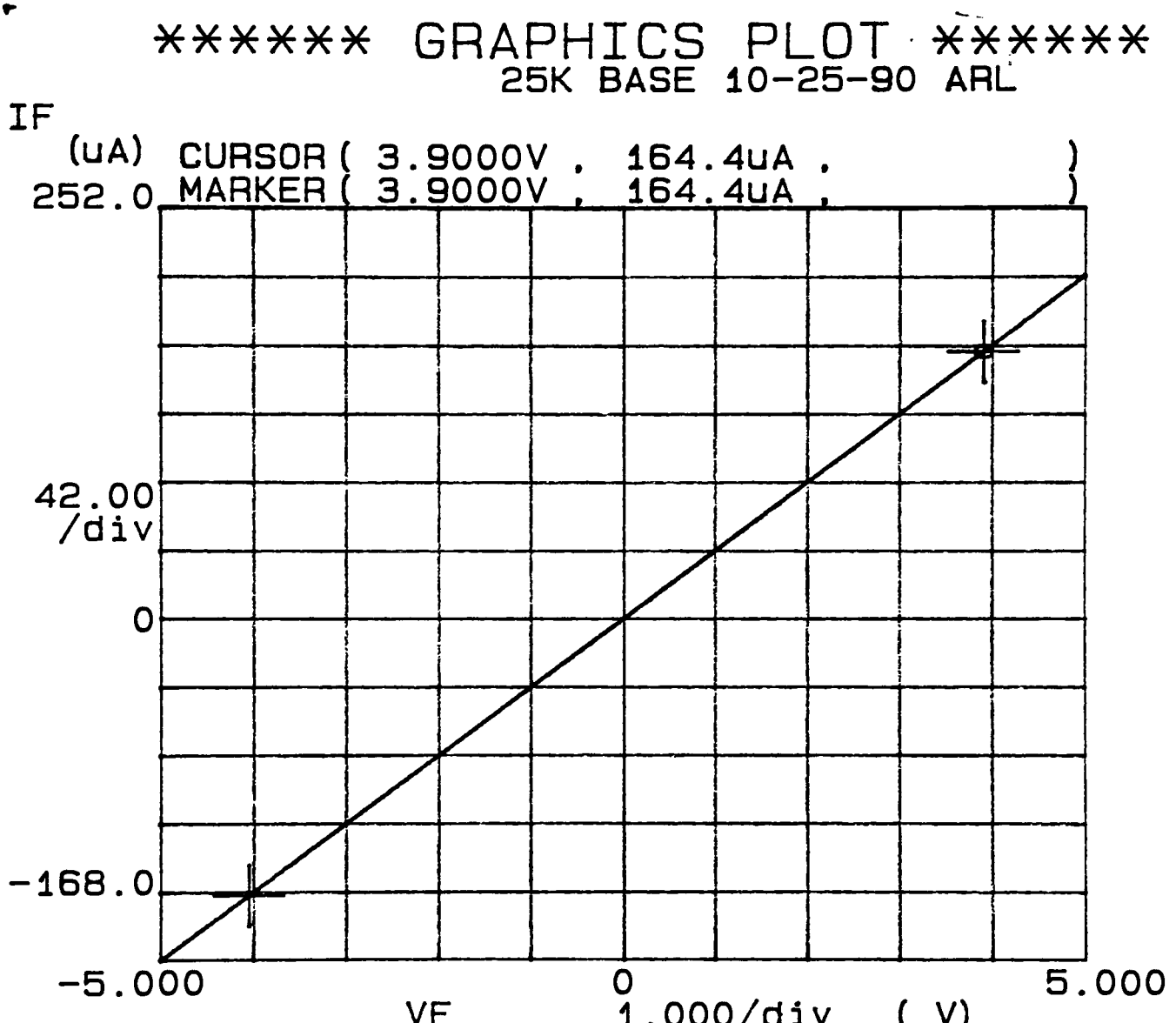
The resistor values were accurate when compared to the design values. Many resistors were tested on several wafers and the results are shown in Table 5.6. While only a sample size of six was used to test each resistor, the measured values are generally within 10-15 percent of the designed values for the base level.

The resistor results were higher than expected. The base resistors were designed with a sheet resistance of 250 ohms per square, but the actual sheet resistance from the

Resistor (ohms)	Mean	Standard Deviation
5.0 k base	4.42 k	969 ohms
18.0 k base	19.45 k	1.41 k
25.0 k base	25.73 k	2.00 k
46.5 k base	48.13 k	5.21 k
1.0 emit	27.5	2.72 ohms
10.0 emit	34.0	3.63
30.0 emit	55.2	7.46
50.0 emit	77.7	5.08
100.0 emit	133.8	17.20
200.0 emit	253.6	26.95

Table 5.6: Resistor results

previous run was approximately 225 ohms per square. The overdesign was done to provide some lattitude in the process since a small number of resistors were tested on the previous run. The increased sheet resistance would again indicate a lower base doping than expected. The emitter resistors also produced higher values than expected. The emitter drive-in diffusion time was extended five minutes during processing, and this would account for the one ohm per square increase in the emitter sheet resistance. Also, the lower emitter doping caused sporadic problems with schottky diodes at the emitter/metal interface. The low value emitter resistors were not close to the designed values, and it was believed that the increase in resistance was due to contact and clubhead resistances which cannot be neglected. The pinch resistors also produced good results, but in a more qualitative sense. Only one pinch resistor had been fabricated on the previous chip, so there was no way to predict a sheet resistance for this device. However, the pinch resistors were expected to



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	42.0E-06	23.8E+03	-13.1E-03	552E-09
LINE2				

Figure 5.7: Sample resistor plots: 25k Base resistor

produce higher results than identically dimensioned base resistors. The pinch resistor sheet resistance was found to be approximately 23.4 kohms per square compared to 250 ohms per square for the base resistors. The pinch resistors did have some non-linearities. Finally, there was some variance in most of the resistor results, and this is apparent by the mean and standard deviation results for each type of resistor. Since these devices are critical in circuit operation this information was promising because the inconsistency was not overwhelming. Figure 5.7 shows a sample plot from the third fabrication run.

CIRCUITS

The current mirror, the differential amplifier and the operational amplifier were the three fabricated circuits that produced operating results. In the first two cases a processing error caused strange results, and in the third circuit modifications were made in order to test the circuit. The current mirror was designed to sink a 200 microamp current, as explained in chapter 4. The measured current ranged between 390 and 525 microamps, as shown in figure 5.8 To test this circuit the supply voltages were kept constant at $\pm$ 5 volts and the voltage at the Q2 collector was varied from -5 to 5 volts. Again, since the voltage drop across the parallel B-E junctions should be identical, the current in Q2 should mirror the biasing current defined by resistor R1. However, if the junctions are not close to perfectly matched

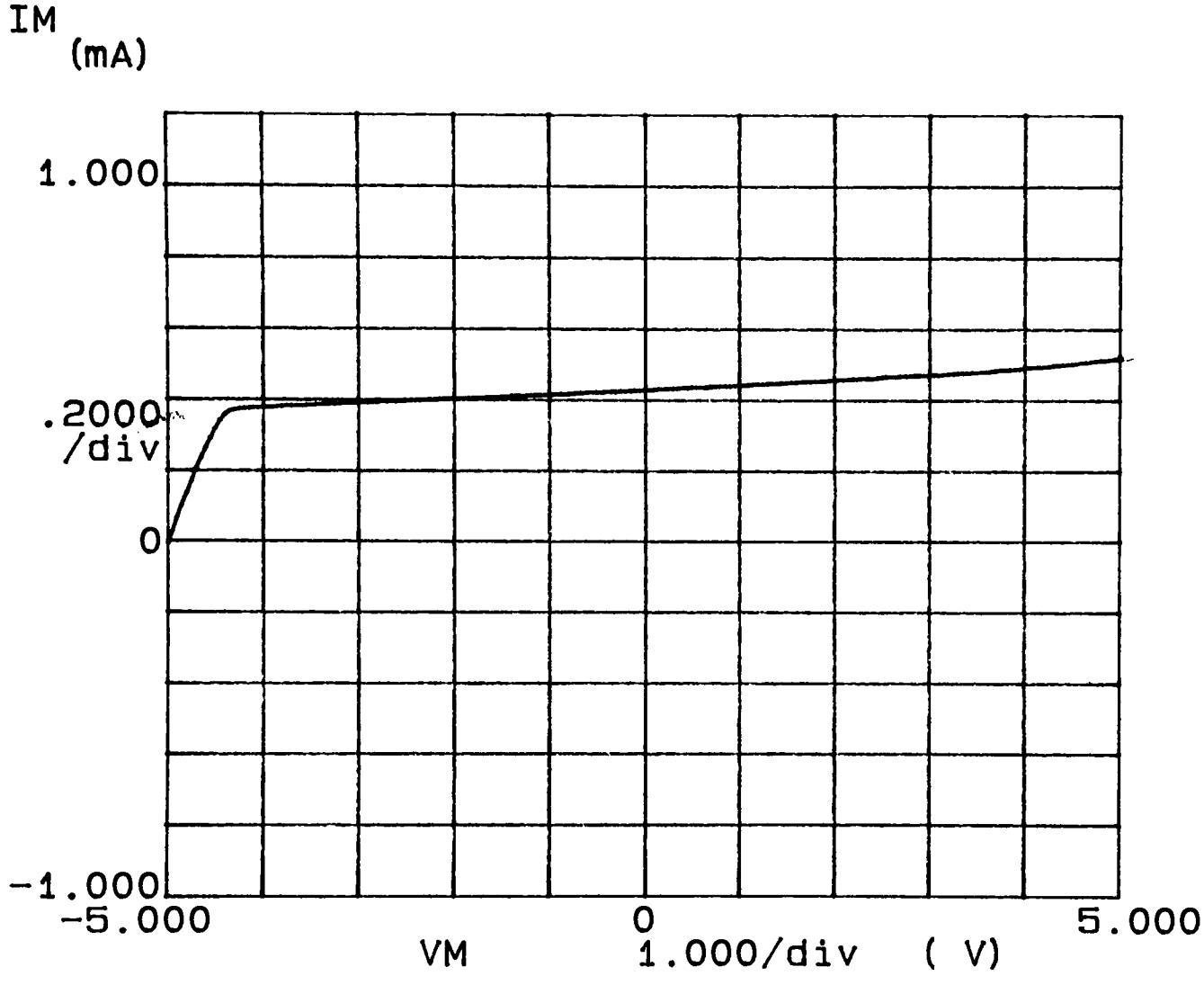


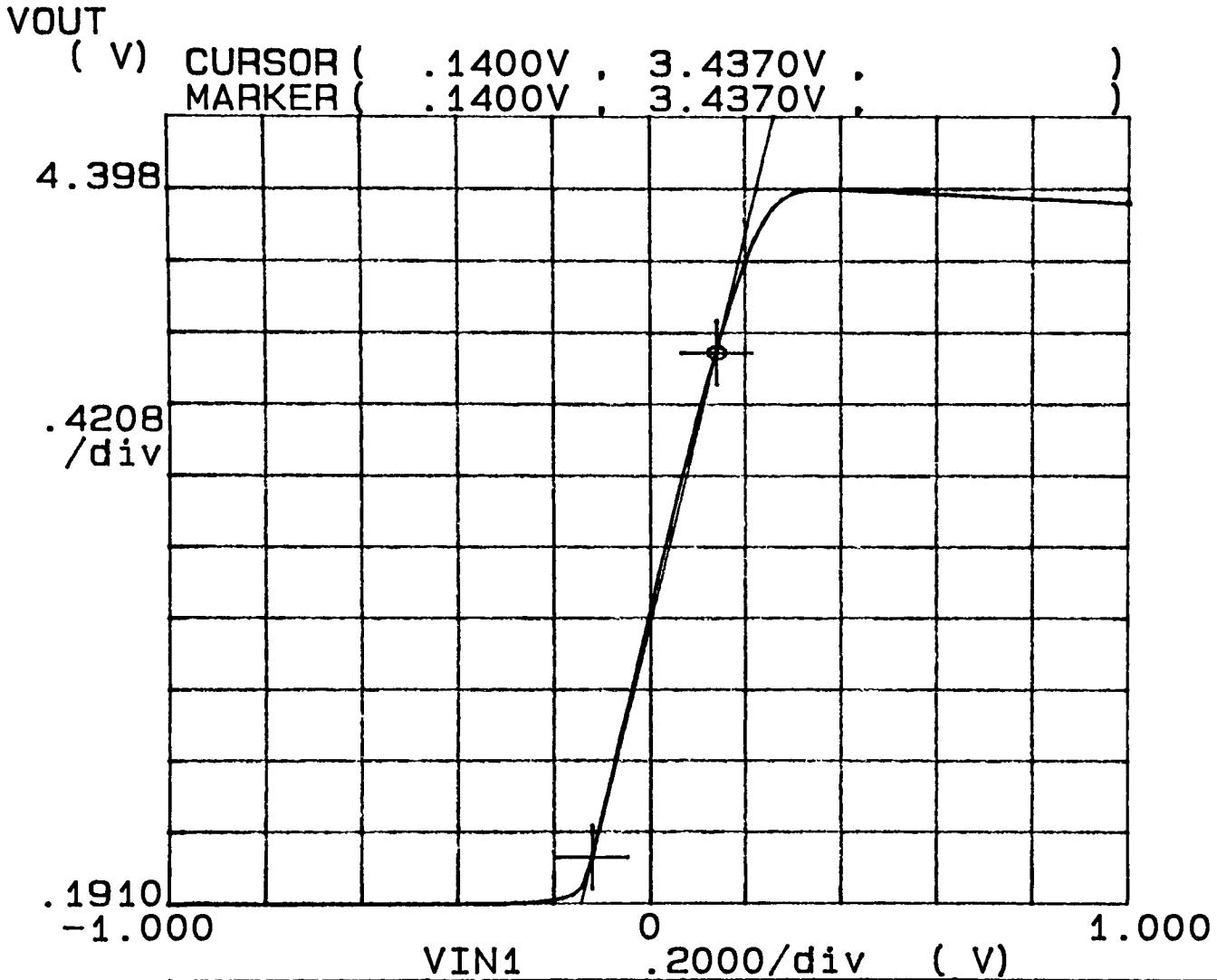
Figure 5.8: Current mirror output plot

the mirrored current will differ from the reference current. In processing terms this means that the base and emitter doping levels must be close to identical.

For the third fabrication run there was a problem with the base diffusion cycle. The solid diffusion source was accidently pushed into the furnace at a high temperature, but should have been pushed in at a low temperature and slowly ramped upward. As a result, the solid diffusion source immediately and non-uniformly doped the device wafers. The manufacturer data sheets state that the slower the deposition the better the deposition uniformity. So, a 30 minute 150^{o}C temperature ramp up cycle was replaced with a 5 minute 950^{o}C cycle, and it was concluded that this error caused the transistor mismatch.

Another circuit that was affected by the mismatch was the differential amplifier, but not to such a great extent. The differential amplifier was tested in a half-differential mode with a single-ended output, and produced a gain of 11.5. This result is shown in figure 5.9 and is typical of several differential amplifiers tested. The SPICE current gain for this circuit was 30.

The circuit was designed to have a biasing current of 200 microamps, but was tested using a 400 microamp source. The current mirror had a 400 microamp sinking ability, and the idea was to simulate the two circuit integration as in the operational amplifier. At the 200 microamp biasing current the differential amplifier output characteristic



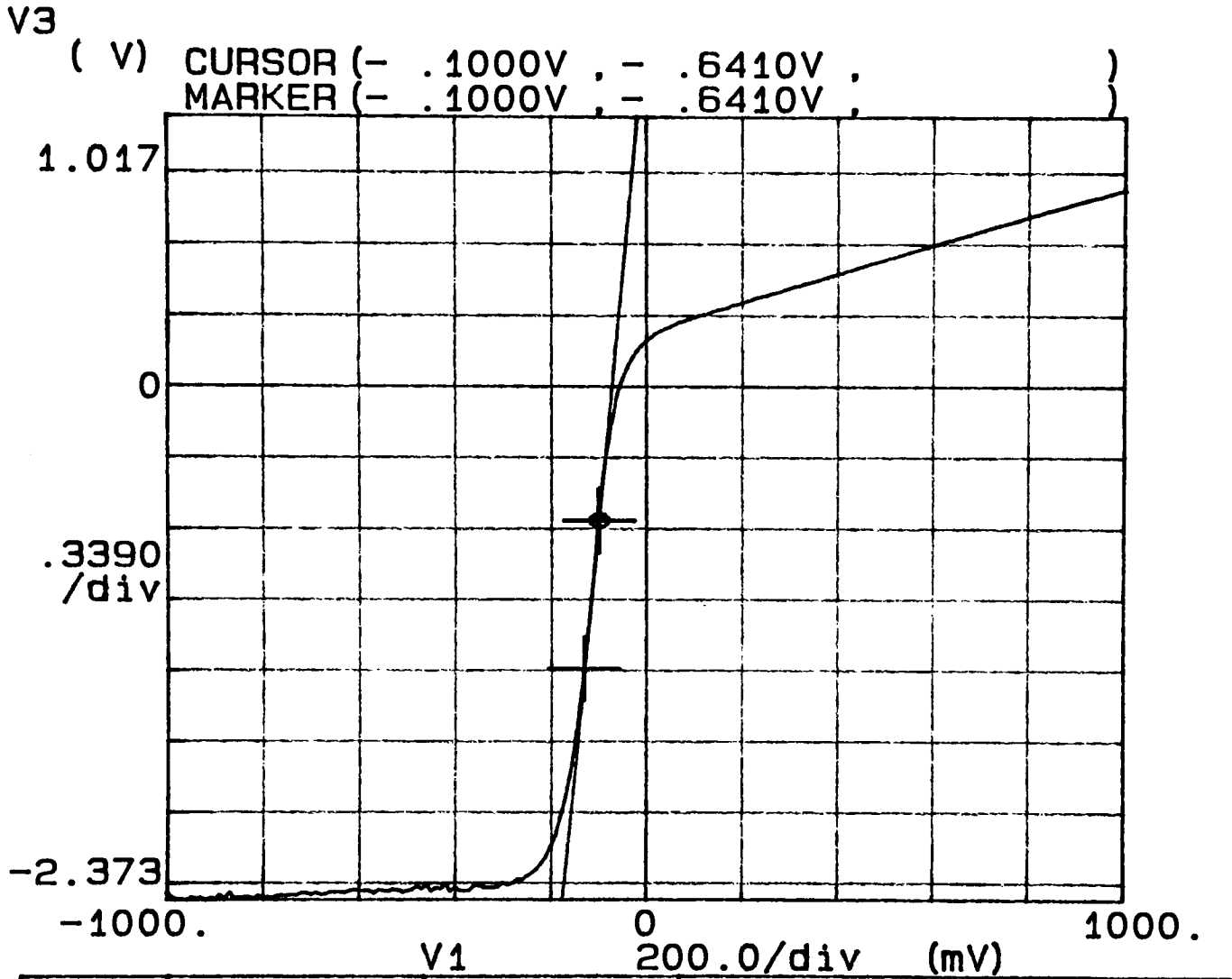
	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	11.5E+00	87.3E-03	-160E-03	1.83E+00
LINE2				

Figure 5.9: Differential Amplifier output curve

approximately similar. The low gain value was again attributed to the transistor mismatch. If the differential amplifier transistors are not matched then the input voltage required for switching may vary over a larger range, and thus lower the change in output voltage to input voltage ratio (i.e. the gain)[8].

The operational amplifier faced two problems: the transistor mismatch and the large PNP transistor failure in the output stage. The transistor mismatch was compounded in this circuit because problem was compounded by the cascaded differential amplifiers and the many mirrored current sources. The failure of the large PNP device was partially circumvented by placing an external 100 kohm external resistor between the output and the negative supply voltage. This at least would allow the positive cycle of the output curve to operate. A probe card was used to test the circuit and out of approximately 400 operational amplifiers tested only two produced a gain over 10. The highest gain was 23.5 and the output curve is shown in figure 5.10. Since the circuit partially operated it is hopeful that with proper fabrication the larger circuits will work in the future.

Four other circuits place on the chip were unsuccessfully tested. A simple inverter circuit using a pull-up resistor was found to have a layout error which prevented the circuit from properly working. An AB ouput stage was also tested, but this circuit utilized the large geometry vertical PNP transistor that had failed previously.



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	23.5E+00	42.5E-03	-72.8E-03	1.71E+00
LINE2				

Figure 5.10: Operational amplifier output characteristic

With each progressive fabrication run changes in the process produced better testing results for devices. The first processing run was experimental and had no theoretical basis. The second run was formulated based on device physics calculations obtained from SUPREM III simulations and "typical" NPN transistor parameters. As a result several working devices were produced including vertical NPN and PNP transistors and a Darlington circuit. The third run attempted to verify the second run results, examine the device operating consistency and expand on the circuit fabrication capabilities. Several devices and circuits were designed, manufactured and successfully tested. These included bipolar transistors, resistors, and small integrated circuits. The lateral active devices necessary for active loads were not successfully fabricated, and a processing error caused some problems with transistor mismatch. Finally, a basic working isolated bipolar process is in place and can be adjusted as required.

CHAPTER SIX: SPICE PARAMETER EXTRACTION

Once the devices were fabricated certain SPICE parameters were extracted from test data. The SPICE parameters were primarily obtained from a vertical NPN transistor using a graph of collector and base currents versus the base-emitter junction voltage and reference 9. The list of parameters and results are shown in table 6.1. These numbers are a combination of extracted, empirical and theoretical values based on processing results. A Hewlett-Packard 4145 Semiconductor Parameter Analyzer was the major testing tool for this exercise.

The first SPICE parameters found were the Transport Saturation Current (I_s) and the Forward Current Emission Coefficient (N_f). The collector current for a transistor is related to the base-emitter junction voltage by equation 6.1.

Eq. 6.1 $$\ln(I_c) = (1/(N_f \times V_t)) \times V_{be} + \ln(I_s)$$

where
- I_c = Collector current
- N_f = Forward Current Emission Coefficient
- V_t = Threshold voltage (.026 volts)
- V_{be} = Base-emitter junction voltage
- I_s = Transport Saturation Current

A linear regression was performed form the values listed in table 6.2 in order to find I_s and N_f. N_f was found to be

SPICE Parameter	Symbol	Value
Saturation current	I_s	58.7 fa
Forward current emission coefficient	N_f	1.0639
Reverse Sat. Current	I_{se}	51.2 fa
B-E leakage coefficient	N_{fe}	1.591
Collector-Emitter forward DC current gain	B_f	100
Early Voltage	V_a	-75 volts
Collector Resistance	R_c	2 kohms
Emitter Resistance	R_e	8 ohms
Base Resistance	R_b	585 ohms
High level injection Roll-off point	I_{ke}	800 uA
Built-in voltage B-E junction	V_{je}	.987 volts
Built-in voltage B-C junction	V_{jb}	.753 volts
Built-in voltage S-C junction	V_{jc}	.662 volts
B-E Junction Capacitance	C_{je}	1.471 pf
B-C Junction Capacitance	C_{jb}	1.720 pf
S-C Junction Capacitance	C_{js}	2.963 pf
Base Transit Time	T_t	.336 nsec

Table 6.1 - Spice parameter results

1.0639 and I_s equal to 58.7 femptoamps. These results were fairly good since the ideal N_f is one and the ideal saturation current is zero amps.

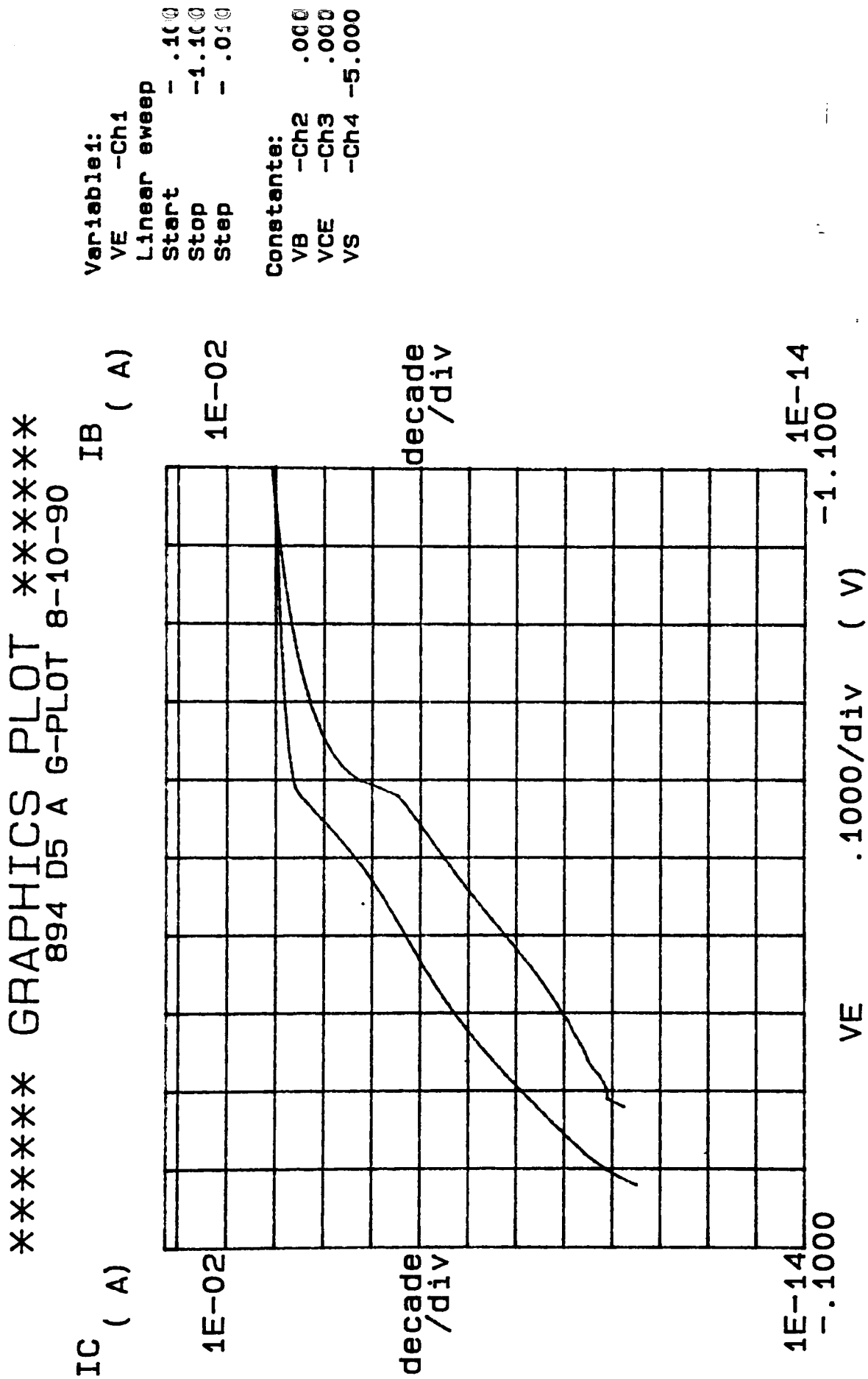


Figure 6.1: I_c and I_b versus V_{be} plot

The same type of analysis was performed for the base current values listed in table 6.2, but to find N_{fe}, the B-E leakage emission coefficient, and I_{se}, the B-E leakage saturation coefficient. The regression results for these two parameters were 1.591 and 51.25 femptoamps respectively. Again these values were acceptable since the leakage emission coefficient was much larger than one, which prevents leakage, and the actual leakage current is small. One note: the V_{be} values used for this analysis were between .20 and .30 volts only for the I_c calculations. This was done because of parasitic resistances that affected the linearity of the curve. The I_b data was extended to .35 volts, but the range as outlined in reference 3 call for V_{be} values between .55 and .66 volts.

The next parameter extracted was $BETA_f$, the Common emitter current gain. Equation 6.2 was used to find Beta over a V_{be} range of .55 to .66 volts. The V_{be} values were used heare because the transistor operated in this region regardless of parasitic resistances.

Eq. 6.2 $$BETA_f = \frac{[(Is)\exp(Vbe/(NfVt)-1)]}{[I_b-(I_{se})\exp(V_{be}/(N_{fe}V_t)-1)]}$$

An average B_f value of 99.99 was obtained over the operating range.

The fourth parameter extracted was V_a, the forward Early voltage. Equation 6.3 and a transistor curve family was used to find V_a.

V_{be} (volts)	I_c (nA)	I_b (pA)
.20	.424	4.50
.21	.609	8.00
.22	.875	11.50
.23	1.258	15.50
.24	1.816	18.50
.25	2.614	23.50
.26	3.772	29.50
.27	5.406	30.00
.28	7.741	45.50
.29	10.99	57.50
.30	15.54	71.00
.31	N/A	87.00
.32	N/A	115.0
.33	N/A	142.5
.34	N/A	184.0
.35	N/A	234.5

Table 6.2: Selected I_c and I_b versus V_{be} data

Eq. 6.3 $$V_{af} = - \triangle V_{bc} \times (I_{c1})/(I_{c2}-I_{c1})$$

where V_{bc} = B-C reverse biasing voltage

I_{c1} = Collector current at V_{bc1}

I_{c2} = Collector current at V_{bc2}

If $\triangle V_{bc}$ is approximated as $\triangle V_{ce}$ then equation 6.3 is a measure of the slope for the family of curves, and where the sloped lines intercept the x-axis is the Early voltage. For the NPN transistor family of curves shown in figure 6.2 the Early voltage was approximately -75 volts.

The next value found was I_{ke}, the high-level injection roll-off point. An approximately value of this parameter was obtained from the I_c versus V_{be} plot of an NPN active mode transistor (see figure 6.1). As the transistor became highly forward biased high-level injection began. This is indicated by the flattening of the curves. The approximate roll-off point is the spot where the curve starts to flatten, and for the curve in figure 6.1 Ike is approximately 800 microamps. To obtain an extact value for I_{ke} a more complicated process was followed which accounted for base resistance and the accompanying V_{be} shift. The more complex method can be found in reference 9. For the present purposes, the approximated roll-off point is an accurate representation of I_{ke}.

Although the base resistance was neglected for the calculation of I_{ke} it was extracted and included in the SPICE parameter list. The base resistance was found using equation 6.5.

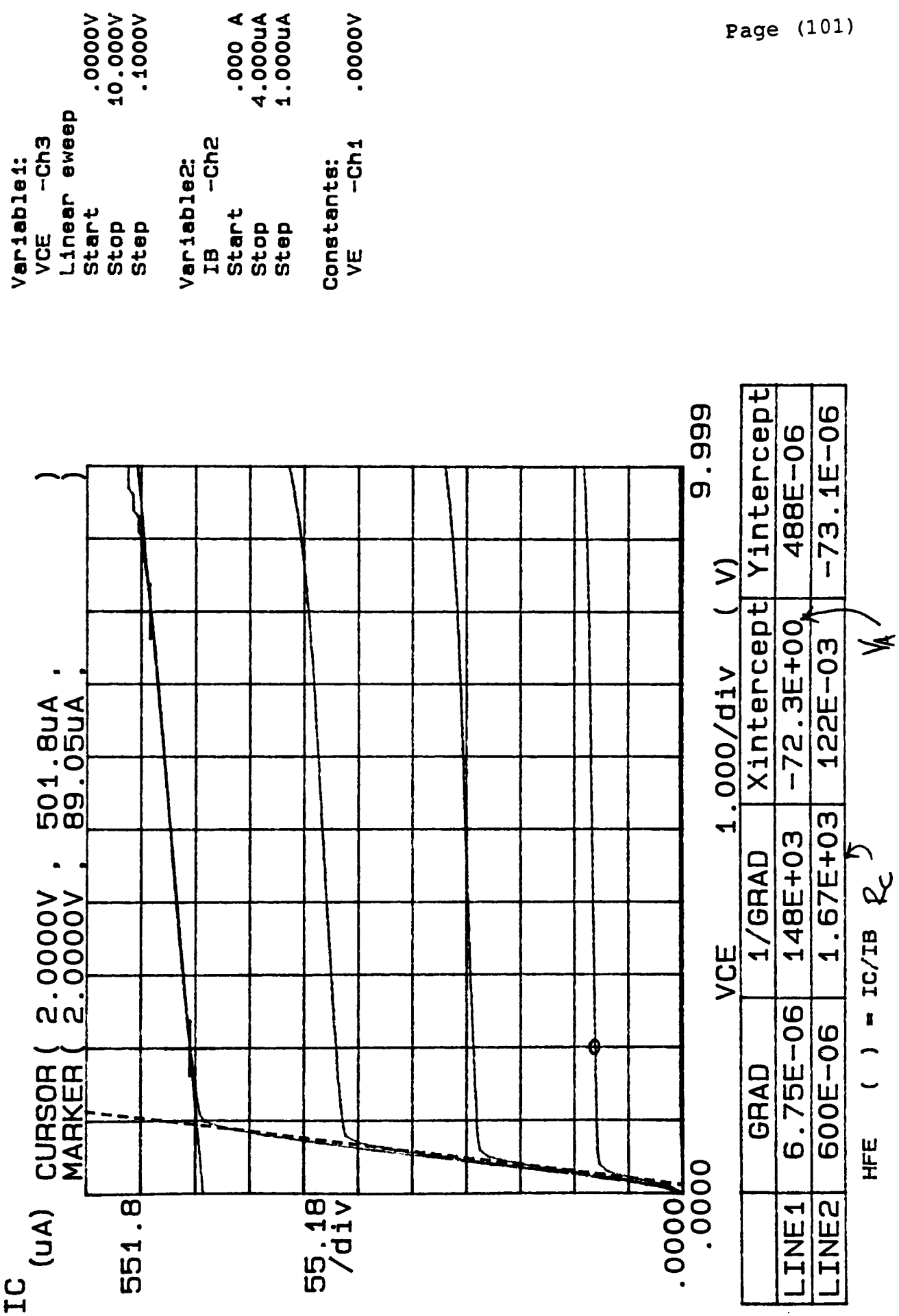


Figure 6.2: NPN transistor characteristic showing Early voltage and collector resistance

Eq. 6.5 $$R_b = [(V_{be} - V_{be'}) - I_c R_e]/I_b$$

where R_b = Base resistance (ohms)

V_{be} = Base-emitter voltage

$V_{be'}$ = Adjusted B-E voltage due to R_b

I_c = Collector current (amps)

R_e = Emitter resistance

I_b = Base current

The I_{ke} value was used for I_c because it essentially remains constant. Therefore, any change in $V_{be'}$ beyond the roll-off point, must be due to base resistance. If no base resistance were present then the base current curve in figure 6.1 would remain a straight line. For the R_b calculation, a V_{be} value was chosen beyond the roll-off point. The low-level injection portion of the curve was extended beyond the roll-off point, and the chosen point was extrapolated back until it intersected the low-level injection line. From this the difference between the ideal and measured Vbe was obtained and used in equation 6.5. This method is shown graphically in figure 6.3 from reference 9.

In order to calculate the base resistance the emitter resistance, R_e, must first be found. The emitter resistance was found using a plot of the base current versus the collector-emitter voltage, and is shown in figure 6.4. The one condition here was that the collector current was to remain at zero amps. As a result, the transistor base

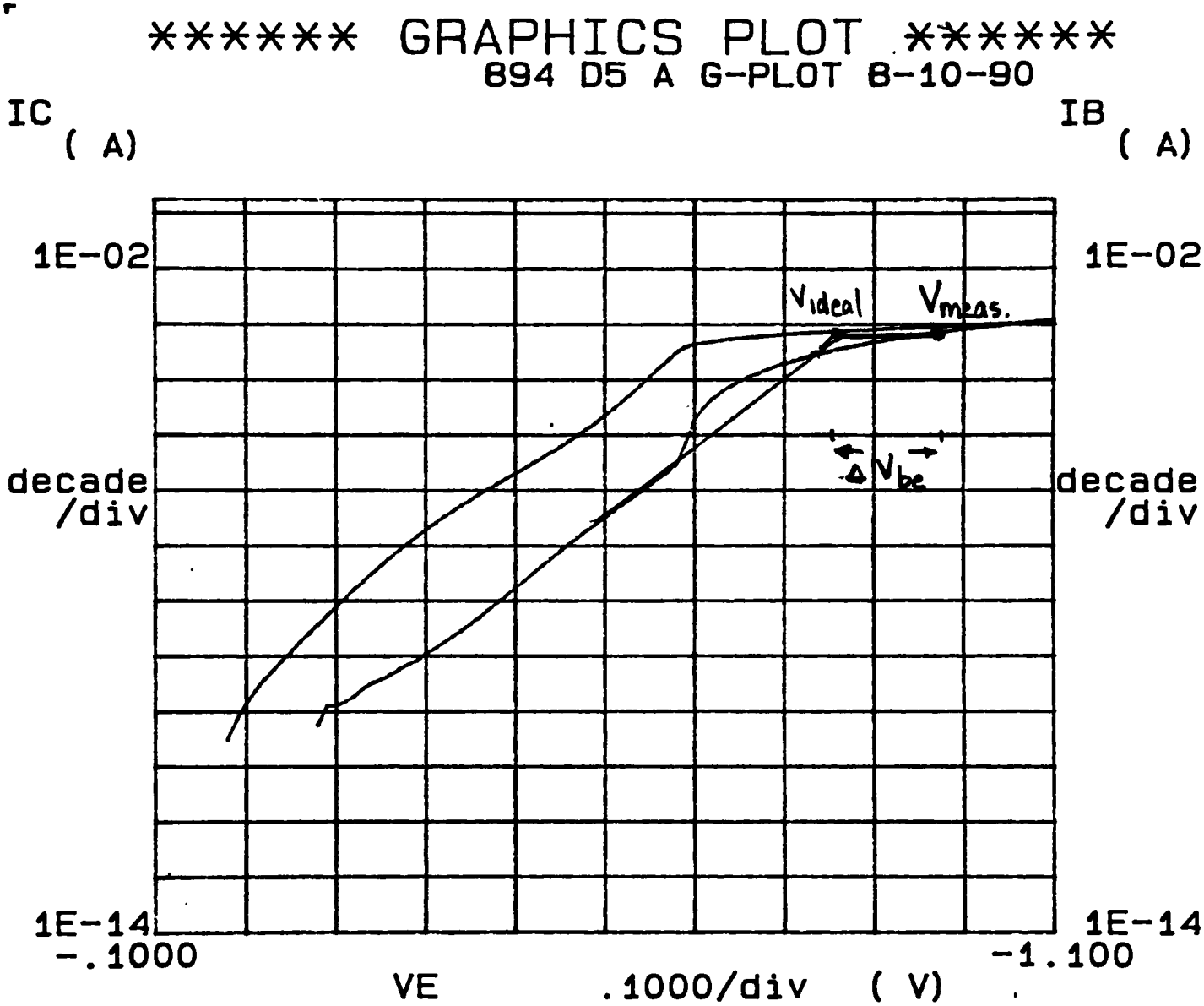


Figure 6.3: Finding the change in V_{be} for R_b calculations

resistance became the slope of the plot. For the transistor shown the base resistance was approximately eight ohms.

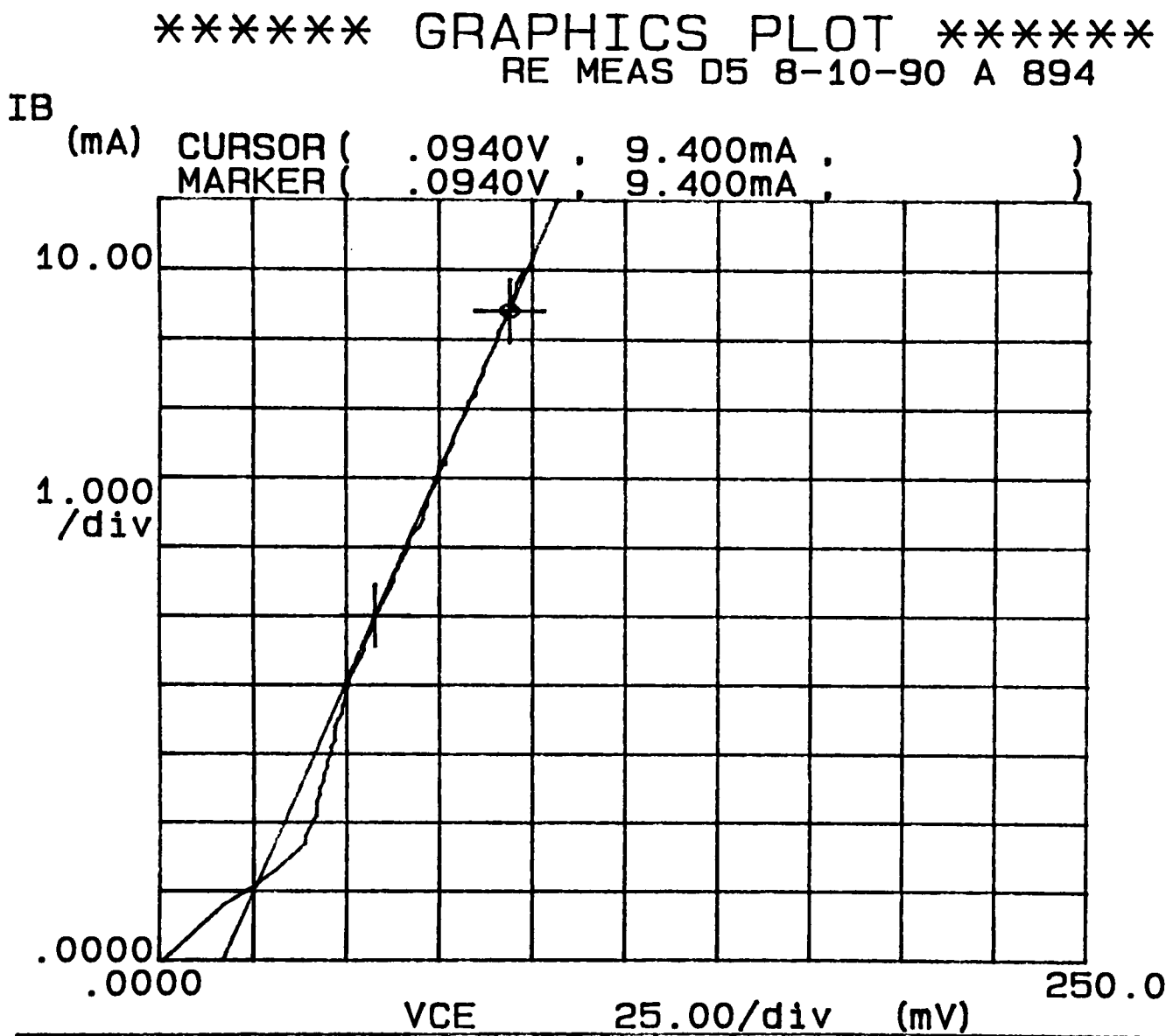
A similar calculation was done to find the collector resistance, R_c. However, the method given in reference 9 did not account for the depletion region extension that occurred without a buried layer. The depletion region extension increased the actual collector resistance. The collector resistance was instead found from the transistor family of curves by measuring the slope of the curves in the saturation region. This is shown in figure 6.2.

The reverse BETA was also a concern. This was found by operating the transistor in the inverse mode and examining the resultant $BETA_f$. The $BETA_f$ in the inverse mode was one, so this was used as $BETA_{rev}$.

The three junction capacitances, C_{be}, C_{bc} and C_{cs}, were included in the list of SPICE parameters eventhough the values were not obtained from measurements. Equation 6.6 was used to calculate the capacitances with processing data on the doping levels.

Eq. 6.6 $$C_j = [(qE_{si}N_aN_d)/(2(N_a + N_d))]^{1/2}$$

All capacitance values were calculated at zero bias and are shown in table 6.3.



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	122E-03	8.18E+00	17.1E-03	-2.09E-03
LINE2				

Figure 6.4: Graph for determining the emitter resistance

Junction	Cj/A (pF/cm^2)	Aj (um^2)	Cj (pF)
B-E	91.95	40 x 40	1.471
B-C	28.67	60 x 100	1.720
C-S	16.59	186 x 96	2.963

Table 6.3: Junction capacitance values

The built-in voltages for each junction were also calculated and included in the SPICE parameter list. The B-E, B-C, and S-C built-in voltages were found using equation 6.7, as shown below.

Eq. 6.7 $$V_{bi} = kt/q \times \ln (N_a \times N_d/(ni^2))$$

The built-in voltages for the B-E, B-C and S-C junction were .987, .753 and .662 volts respectivevly. Finally, the base transit time, or average time for minority carriers to traverse the base, was determined using equation 6.8.

Eq. 6.8 $$T_t = W_b^2/(2D_x)$$

where T_t = Base transit time (seconds)

W_b = Electrical basewidth (cm^2)

D_x = Carrier Diffusivity in base (cm^2/sec)

The base transit time using a basewidth of 1.1 microns, and diffusivity of 20 cm^2/sec was .336 nanoseconds.

A number of SPICE parameters were obtained for an NPN vertical transistor. Many of these can be used to derive a SPICE model for other devices such as PNP vertical transistors and JFETs. While most are DC parameters they provide a basis from which to model circuitry using SPICE and obtain more information on both the circuits and the devices.

CHAPTER SEVEN: CONCLUSIONS/RECOMMENDATIONS

In the course of developing the RIT N-Well Bipolar fabrication service several successes have evolved. However, to have a complete and manufacturable process improvements are required. These consist of minor process changes and design alterations.

CONCLUSIONS

A bipolar process has been established. The best NPN vertical transistors produced a gain of 100 with a breakdown voltage of approximately 15 volts, a Early voltage of -75 volts, and a 2 kohm collector resistance. The best vertical PNP transistors had a gain of 40, a breakdown voltage greater than 30 volts, and a very large Early voltage. One drawback to these devices was the non-isolated collector, and a major question with both NPN and PNP devices was the consistency of operation. Only 9 of 10 transistors had similar operating characteristics. This poses problems for manufacturing large circuits. In addition the large geometry PNP transistors did not operate due to high base resistance. Both lateral NPN and PNP devices did not produce acceptable results, and the main problem was the low gains produced. The lateral NPN gain was one and the PNP gain was .25. Without these isolated transistors, circuits using PNP active loads and non-resistor levelshifting is impossible.

Resistors were used to offset transistor limitations, and the fabricated results were promising. The Base level resistors were generally within 15 percent of predicted values using a sheet resistance of 250 ohms/square. The emitter level resistors produced higher than expected results due to processing changes, but provided consistent resistor values. At low resistor values, less than 30 ohms, the clubhead and contact resistances dominated resistor values, and schottky diodes at the emitter resistor contacts presented a sporadic problem with operation.

Several small circuits worked on the third fabrication run, but a processing error produced unexpected results. Current mirrors provided a current twice the designed value, and differential amplifiers had a lower gain than expected. Transistor mismatch due to non-uniform base doping was attributed to these results. The operational amplifier failed because of this mismatch and a large geometry PNP output transistor. On the second fabrication run a working NPN Darlington circuit was produced that had a gain in the thousands.

Other miscellaneous devices placed on the testchips did not fair well in the test lab. The threshold voltage shifts for the PMOS and NMOS transistors was in the 20 volts range, and this was mainly laid on the wet gate oxide that the devices used. The JFETs failed to pinch the channels shut. It was believed that the base doping level was high enough to prevent the necessary depletion region extension needed to

pinch the channel shut. This was expected because the vertical NPN transistors were designed to prevent this effect using the same three layers (emitter, base, N-well).

From the vertical NPN devices a number of SPICE parameters were either extracted or derived. Many of these parameters can be extended to other devices such as the vertical and lateral transistors. The parameters obtained include collector-emitter short circuit current gain, Early voltages, parasitic resistances on all doping levels, saturation currents, built-in voltages and junction capacitances.

To assist designers wishing to use bipolar circuitry a small standard cell library was formed using ICE. Included in the library were NPN and PNP transistors, MOS transistors, various base and emitter level resistors, and some test structures. From the simple cells larger standard cells such as a Darlington circuit, a current mirror, an AB output stage, a differential amplifier and an operational amplifier were designed. These cells were put together along with basic design rules and an ICE information and formed into a Users guide for the RIT N-Well Bipolar fabrication service.

RECOMMENDATIONS

To have a completely working and MANUFACTURABLE process several items need to be addressed. Some of these issues are mentioned below with some possible solutions, including plans extending beyond this process.

1). To have working lateral PNP transistors the base width must be less than the present 6 microns. To do this the designed basewidths of 10 microns must be reduced to nine, eight, seven and six microns to provide final basewidths of five, four, three and two microns respectively. The small basewidths will help offset base and surface recombination effects.

2). To obtain better MOS devices (for BICMOS) the contact cut oxide should be grown with a dry oxide as for most MOS gate oxide. The forward Beta may decrease in the bipolar devices, but this should be minimal.

3). To increase repeatibility and uniformity in the transistors and resistors the solid source diffusion times should be increased to at least 30 minutes, as recommended by the manufacturer. If the process alterations are done to provide identical doping levels and junctions depths the device operating characteristics should remain the same.

4). Once the process is redesigned the SPICE parameters should be extracted for all devices.[3]

5). The emitter doping level should be high enough to eliminate schottky diode contact effects. A doping level of 8×10^{19} Atoms/cm^3 should be high enough.

6). AC prediction and testing should be performed on devices and a small signal model formed for better design capabilities

7). In the interest of making a BICMOS process the diffusions could be replaced with implants to allow an easier transition into BICMOS.

8). An effort to obtain accurate lifetimes should be made. Presently, a lifetime of .1 microseconds is used based on very sketchy test information.

9). Special SUPREM III models should be defined for the solid diffusion sources. This would assist in accurately modelling process simulations.

ACKNOWLEDGEMENTS

I'd like to thank Dr. Lynn Fuller for his initial idea of the fabrication service and for his guidance along the way. I'd also like to thank Dr. I Renan Turkman for his assistance with the physics and review of the second chapter of this thesis. Similarly, I'd like to thank Professor Robert Pearson for his contributions and the rest of the RIT Microelectronic Engineering department for their support. A special thanks to Mr. Scott Blondell and his staff for their marvelous help with the processing equipment, especially the Ion Implanter. To Digital Equipment Corporation, for funding me in graduate school, and Miss Tamera Slavik for performing a significant portion of the first processing run, a thanks as well. Finally, I'd like to thank Mrs. Julie A. Lazeski, who pushed when I needed a push, encouraged when I was discouraged, and helped me reach my goal.

APPENDIX 2.1

RIT N-WELL FACTORY PROCESS

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RIT N-WELL BIPOLAR FACTORY PROCESS

Step	ID	Description	Information	Wafers
01	IDN01	Scribe & Res.	--------	All
02	CLE02	RCA Clean	--------	All
03	OXI05	N-Well Oxide	1100C, 25 Min 5 l/m O2, 3500 A	Device, C1
04	NAN0	SiO2 meas.	--------	C1
05	ETC01	Step etch	3500 A	C1
06	PHL01	Photolith	mask #1, N-well	All Device
07	ETC02	SiO2 etch	3500 A	All D, C1
08	IMP01	Ion Implant	Phosphorous 8E12 Dose, 110Kev	All Device & C1-C4
09	ETC07	Resist Strip	--------	All Device
10	CLE02	RCA Clean	--------	All D, C1-C4
11	OXI08	SiO2 growth	1150C, 8 Hours 7500 A	All D, C1-C4
12	OXI08	N-well drive	1150C, 40 Hours N2, 2 l/m	All D, C1-C4
13	NAN0	SiO2 meas.	---------	C1
14	ETC01	Step etch	7500 A	C1
15	DET02	Restvty meas.	---------	C1
16	GRV01	Junction depth	---------	C1
17	CLE02	RCA Clean	---------	All Device
18	PHL02	Photolith.	mask #2, base	All Device
19	ETC06	SiO2 etch	7500 A	All D, C2,C3
20	ETC07	Resist etch	--------	All Device
21	CLE02	RCA Clean	--------	All D,C2,C3,C5
22	DIF03	Boron Dep.	10 min., 950 C	All D,C2,C3,C5
23	NAN0	BSG meas.	--------	C2
24	OXI04	LTO	25 min., 750 C O2, 5 l/m	All D,C2,C3,C5
25	NAN0	LTO meas.	--------	C2
26	ETC06	LTO etch	130 A	All D,C2,C3,C5
27	CLE02	RCA Clean	--------	All D,C2,C3,C5
28	OXI04	Base Drive	30 min 1100C 5 l/m	All D,C2,C3,C5
29	OXI05	Base Drive	20 min 1150C 5 l/m	All D,C2,C3,C5
30	NAN0	SiO2 meas.	--------	C2
31	ETC01	Step etch	4500 A	C2
32	PHL02	Photolith	Mask #3, emitter	All Device
33	ETC06	SiO2	4500 A	All D,C2,C5
34	DET02	Restvty meas.	--------	C2
35	GRV01	Junction depth	--------	C2
36	ETC07	Resist etch	--------	All Device
37	CLE02	RCA Clean	--------	All D,C3,C4
38	DIF03	Phos. Diff.	20 min., 975C, N2	All D,C3,C4
39	ETC02	SiO2 etch	--------	All D,C3,C4
40	TES01	Beta Test	--------	D2, D5
41	CLE02	RCA Clean	--------	All D,C3,C4

42	OXI04	Phos. Drive	15 min,1050C,5 l/m	All D,C3,C4
43	NAND	SiO2 etch	--------	C3
44	ETC01	Step etch	--------	C3
45	PHL02	Photolith	Mask #4, cc	All Device
46	ETC06	SiO2 etch	1000 A	All D,C3,C4
47	ETC07	Resist strip	--------	All Device
48	CLE02	RCA Clean	--------	All D, C5
49	MET01	Alum. Dep.	2-3 pellets	All Device
50	PHL01	Photolith	Mask #5, metal	All Device
51	ETC05	Al etch	--------	All Device
52	ETC07	Resist etch	--------	All Device
53	SIN01	Sinter	20 min,450C,H2N2	All Device
54	TES01	Test	--------	All Device

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ESTABLISHING AN N-WELL BIPOLAR FABRICATION SERVICE AT RIT

APPENDIX 2.2

SOLID DIFFUSION SOURCE PROCEDURES

INTRODUCTION

Silicon based IC technology is dependent on solid state diffusion to control impurity concentration and distribution in a semiconductor substrate. The diffusion process typically involves two steps; first, the deposition (or prediffusion) of impurity atoms and second, the redistribution (or drive-in) of the impurity atoms. The deposition step is critical since it controls the amount of impurity atoms introduced to the silicon substrate. Dopant uniformity across a wafer and across the lot, measured through variations in sheet resistance, is established during this first step in the diffusion process. Improvements in the doping process are made by improving the control of the impurity transfer at the deposition step [1].

The undergraduate microelectronic facility at The Rochester Institute of Technology is currently restricted to impurity doping of semiconductor substrates from spin-on sources. This method of diffusion introduces the dopant to the silicon wafer through a thin dopant film. Controlling the amount of impurity diffused into the the silicon substrate is difficult since the wafers are not at thermal equilbrium within the furnace prior to being exposed to the dopants. This method, although safe, has not been dependable in diffusing controlled amounts of impurity atoms into a host substrate. Problems with the spin-on sources, in both uniformity and reproducibility, have plagued the students ability to fabricate working devices on a consistent basis.

Conventional thermal diffusion, based on a carrier gas system, poses hazardous safety problems. The dopants in this type of system, found in liquid and gaseous forms, are toxic, highly poisonous, and corrosive (see Table 1). These compounds undergo oxidizing reactions and thermal decomposition at a given diffusion temperature resulting in additional toxic and corrosive by-products. Expensive scavenger and scrubber systems must be installed to collect these compounds in order to prevent operator exposure and insure environmental safety. The benefits of satisfactory sheet resistance uniformity and lot-to-lot repeatability do not offset these safety concerns.

COMPOUND	FORMULA	PHASE	PROPERTIES
Phosphine	PH_3	gas	Very toxic, flammable
Phosphorous Oxychloride	$POCl_3$	liquid	Poisonous,corrosive
Boron Tribromide	BBr_3	liquid	Very toxic, corrosive
Boron Trichloride	BCl_3	liquid	Very toxic, corrosive
Diborane	B_2H_6	gas	Very toxic, flammable

Table 1
Properties of Carrier Gas Dopant Sources

An alternative to the spin-on impurity system and carrier gas system is diffusion from an ion implanted layer. Ion implantation provides precise control of the total dopants (from 10^{14} cm^{-3} to greater than 10^{21} cm^{-3}) introduced into a semiconductor substrate [2]. The process of diffusion

occurs during the high temperature anneal required to electrically activate the implanted impurity atoms and repair the crystal damages inherent to the implantation process. The facility at RIT will soon have the capability and the benefits of ion implantation; however, because of the equipment's limitation of low through-put and the lack of technical expertise required to operate and maintain such a piece of equipment its use will be limited.

The planar diffusion source (PDS) system of diffusion offers a safe solution to the uniformity and repeatability problems associated with the spin-on sources, the potential hazards accompanying the carrier gas system, and the shortcomings related to ion implantation. The PDS system, a product of Sohio Engineered Materials Company, uses wafer shaped disks of phosphorous and boron compounds as n-type and p-type impurity sources respectively. During a diffusion cycle the dopant species associated with each source volatilizes directly from the surface of the source wafer. An inert gas, such as nitrogen, is flowing during the diffusion process to prevent the back flow of contaminants into the diffusion tube, and to insure the formation of a boundary layer around the periphery of the stacked source and semiconductor wafers. The gas flow does not act as a carrier to the dopants. The dopants vaporizing from the source wafer diffuse through the static region between the source wafer and the semiconductor substrate. Because of the absences of any turbulent flow, sheet resistance uniformity can be controlled within ±2% across an individual semiconductor wafer and within ±3% across a boat of wafers [3].

The compounds which make up the PDS system of diffusion are silicon pyrophosphate (SiP_2O_7) and boron nitride (BN). Each source, although similar in appearance, requires different processing procedures in order to be used as a high-performance method of diffusion. The bulk of this report will be an introduction to the PDS system of diffusion, describing in detail the proper handling, activation, and diffusion techniques required to correctly use these sources.

CHAPTER I

THE PDS-PHOSPHOROUS SYSTEM

System Reactions

There are three types of phosphorous sources; PH-950, PH-1000N, and PH-1025. Each source consists of the active component silicon pyrophosphate (SiP_2O_7) and a binder. The difference between each source is in the mixture ratio of the two components. Therefore, a PH-950 source consisting primarily of silicon pyrophosphate is active in a lower temperature range than either PH-1000N or PH-1025 sources.

Dopant transfer occurs when the silicon pyrophosphate thermally decomposes generating the dopant species phosphorus pentoxide (P_2O_5). Phosphorous pentoxide evolves from the source by direct volatilization while silicon dioxide, a by-product of the reaction, remains on the source wafer. At room

$$SiP_2O_7 + \text{heat} \longrightarrow P_2O_5 + SiO_2 \qquad (1)$$

Ref. 4.

temperature the dopant species P_2O_5 is a glass with a characteristic melting point at 360°C. The diffusion ambient allows P_2O_5 to exists in its vapor state; thus, promoting the mass transfer of the dopant along a concentration gradient between the source and silicon wafers.

Fick's first law (Eq. 2) describes the movement of the dopant to the silicon wafer, where J is the diffusion flux of the dopant species, a; D_{ab} is the diffusivity of a through the ambient b; C_a is the molar concentration of a; and x is a distance coordinate. A stationary medium between

$$J = -D_{ab}(\delta C_a/\delta x) \qquad (2)$$

the source and silicon wafers exist due to the stacking arrangement in the source boat. The high rates of vaporization and the short distance that the dopant must transfer lead to the rapid attainment of the impurity solid solubility limit within the silicon. The ambient in which the dopants are transferred is free of turbulent motion since no carrier gas is used. Variations in sheet resistance can be controlled within ±2% across a wafer and within ±3% across a run.

Source Preparation

Prior to any diffusion each source must be properly activated. The activation procedure for each of the phosphorous sources is a thermal anneal as describe in Table 2. The purpose of the activation cycle is to alleviate stress in the host substrate and remove residual moisture retained by the source.

The activation procedure may be carried out several times during the lifetime of a source. If a source has not been used for several weeks or has been removed from the diffusion furnace it must be reactivated prior to its use. Overnight storage in a dry box or diffusion furnace at 500-700°C requires a 1 hour anneal at the process temperature. The practice of reactivation and daily anneal allows the user to establish rigid specification for the process.

ramping. A base temperature at which all deposition cycles begin is 800°C. The sources are not active at this temperature so no dopant transfer will occur. During the ramping step the temperature within the furnace will approach the lower temperature limit of the source; set at 75°C below a source's designated temperature limit. At this point the active component in the source will begin to brake down and generate the volatile dopant species P_2O_5. Once the soak temperature is reached the rate of dopant vaporization will be at maximum promoting the dopant transfer along the concentration gradient between the source and the silicon wafer.

·PDS-Phosphorus
Activation / Deposition

STEP	TEMP (oC)	TIME (min)	GAS
Push & Recovery	800	30	dry N_2 (5 slpm)
Ramp-Up	800 - xxx	5 °C/min	dry N_2
Soak	xxx	***	dry N_2
Ramp-Down	xxx - 800	10 °C/min	dry N_2
Pull	800	15	dry N_2
Storage	600		dry N_2 (2 slpm)

(xxx, *** - predetermined process temperature and time dependent on the desired sheet resistance.)

Table 3

Upon completion of the soak step, the furnace controller will begin to return the furnace to the base temperature of 800°C. This step in the sequence is critical, since the impurity atoms will continue to diffuse in the silicon substrate effecting the final sheet resistance and junction depth. Table 3 suggests a cool down rate of 10°C/min; however, the furnace's natural cooling rate will be the determining factor effecting this parameter (see Appendix A).

Once the wafers are pulled from the furnace and the run is complete, precautions must be taken to store the sources correctly. The most effective storing procedure is to return the souces to the furnace at a reduce temperature and gas flow of 600°C and 2 slpm respectively. Storing the sources in this manner eliminates the threat of moisture damage caused by humidity changes in the laboratory. If the furnace capacity is not available, storage in an oven or dry box is also acceptable. In any case, prior to reusing the sources each must be annealed for at least one hour at the process temperature. Extended periods were the wafers are not in use will require a complete reactivation. It is not uncommon to repeat the activation cycle several times in the lifetime of a source.

Process Evaluation

The average glass transfer, the average sheet resistance, and the impurity profile junction depth are the three parameters used in the evaluation of the deposition cycle. The average thickness of the P_2O_5 glass deposited onto a silicon wafer is determined through ellipsometery using a refractive index value of 1.50. The average sheet resistance of the diffused layer can be determined with a four point probe after the test wafers have been deglazed. Since the deposited impurity layer is a glass dipping the wafers in a 10:1 solution of HF will expose the bare silicon surface. When measuring the sheet resistance of a phosphorus diffusion it is important to take the sheet resistance

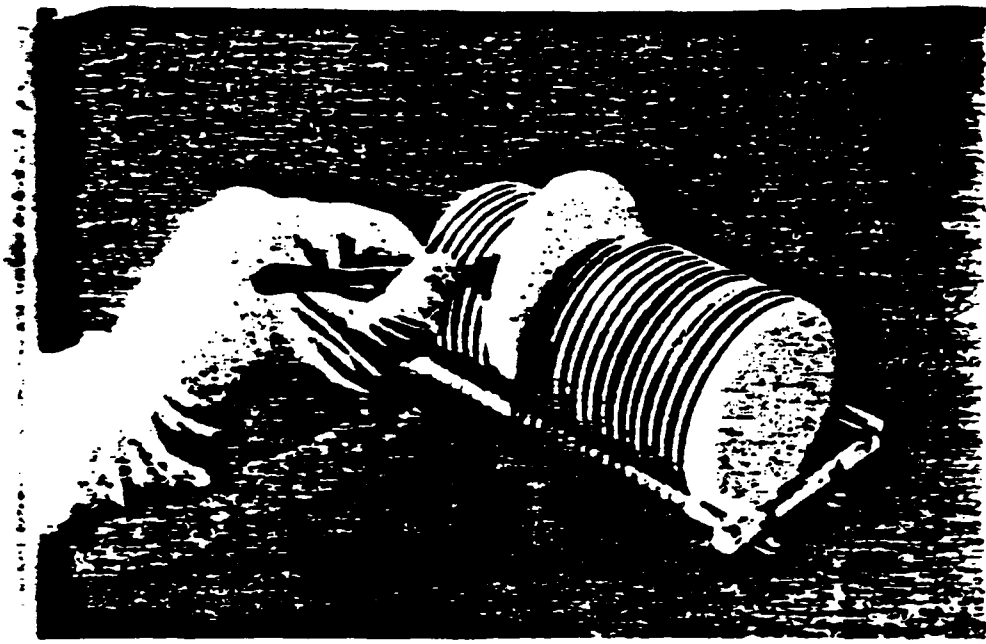
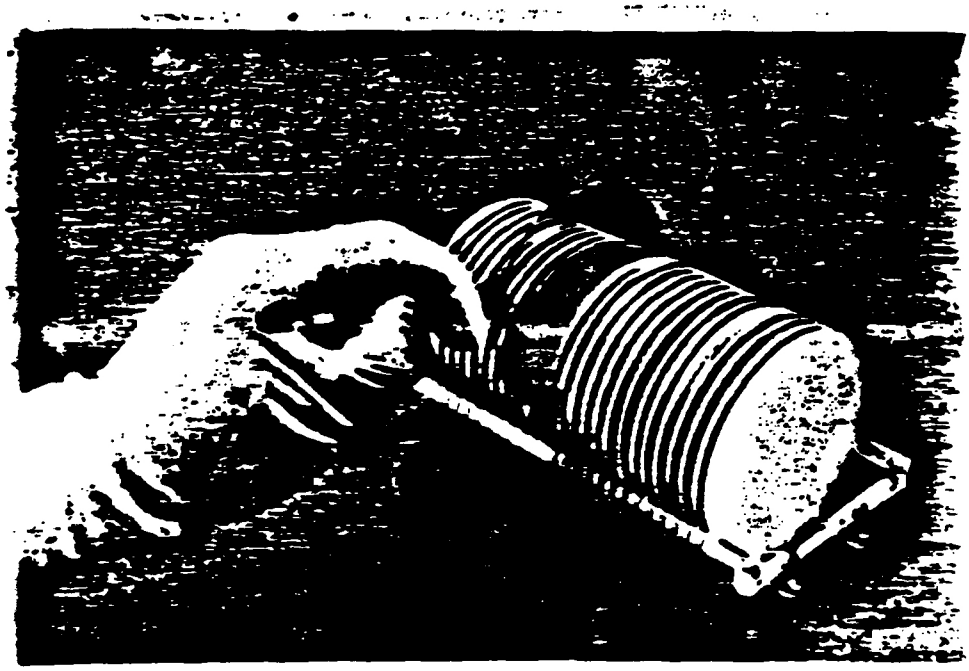


Figure 1-1A



BOTH SOURCE WAFERS AND SILICON WAFERS CAN BE LOADED INTO QUARTZ BOAT USING TWEEZER.*

Figure 1-1B

* Figures 1-1A and 1-1B were supplied by James R. Dalcin Applications Engineer for Standard Oil's Engineered Materials Group.

readings in the dark or have the probe head covered with a black box to prevent erroneous readings caused by the photogeneration of carriers. The simplest and quickest way to determine the impurity junction is through the grove and stain technique (see Appendix B). Although this method is destructive it is accurate within ±1% for junctions ≥ one micron [5].

The collection of this data should be recorded for the specific run and also logged in a record book for lifetime studies of the source. When used correctly, any source can last approximately 500 hours of processing time. Indications that a source is depleted will show up in lower glass transfers and higher sheet resistance readings for a standard deposition cycle. Once a source is depleted it is no longer need and can be discarded in a waste bin.

CHAPTER II

PDS-BORON NITRIDE

System Reactions

The boron nitride system is dependent upon the oxidation of the boron nitride (BN) source to supply the volatile dopant compound boron oxide, B_2O_3. The thin layer of B_2O_3 glass formed over the source wafer will act as the dopant source during the subsequent deposition process.

$$4BN + 3O_2 \longrightarrow 2B_2O_3 + 2N_2 \quad (3)$$

$$B_2O_3 + \text{heat} \longrightarrow B_2O_3\ (\text{vapor}) \quad (4)$$

Alone, the BN source is chemically stable at the deposition temperatures ; therefore, to achieve repeatable control, the B_2O_3 layer must be regenerated and stabilized prior each deposition cycle.

Similar to the n-type sources there exits three grades of p-type sources; BN-975, BN-1100, and BN-1250. The difference between each source is the BN to binder ratio, with the binder being composed mostly boron oxide. As with the phosphorous sources, the designation number assigned to each source indicates its upper temperature limit. Using a source out of the suggested temperature range will result in a degradation of sheet resistance uniformity in addition to shortening the lifetime of the source.

The basic principles of planar source diffusion as an in-situ dopant source for silicon IC fabrication are similar for both phosphorus and boron systems. However, the chemistry of each system is quite different considering the phosphorus source requires little maintenance other than periodic reactivation due to sporadic use. In contrast, the boron nitride (BN) sources require constant maintenance in order to regenerate the dopant oxide layer. This difference results in slightly more complex handling procedures for the BN sources. The preceding sections will elaborate on the proper techniques required to use the BN planar source effectively.

Source Preparation

Prior to any diffusion each source must be properly activated and stabilized. The activation procedure generates a layer of boron oxide from the thermally stable boron nitride source. During a subsequent deposition cycle the dopant layer will evaporate from the surface of the source wafers depositing itself on adjcent silicon wafers.

Stabilization is a thermal anneal after activation. The purpose of the stabilization is to achieve a uniform layer of dopant glass across the source wafer. Stabilizing the source after activation and prior to any subsequent diffusion assures rigid sheet resistance uniformity and lot to lot repeatability. Tables 4 and 5 show the proper activation cycles for the BN sources.

Included in each activation procedure is a dry bake. This step will remove residual background moisture from the system. The oxidized boron nitride source is sensitive to moisture and ambient humidity. Boron oxide in the presence of water vapor will react to from metaboric acid (Eq. 5). The vapor pressure of the metaboric acid is significantly higher than that of the boron oxide. This higher vapor pressure leads to a higher diffusivity of a boron rich compound making

the predeposit process difficult to control . The mechanics of this reaction are favorable when the moisture level in the system can be controlled. An alternative process known as the "hydrogen-injection" process utilizes the above reaction to obtain significant improvements in dopant transfer. The "H2-injection" process will be discussed in the next chapter of this report.

METABORIC ACID

$$B_2O_3 + H_2O \rightarrow 2HBO_2 \qquad (5)$$

BN-975
Activation / Stabilization

STEP	TEMP (oC)	TIME (min)	GAS
Bake	350-400	60-90	dry N2
Oxidation	900-950	30	dry O2
Stabilize	At Use Temp.	30	dry N2
Storage	350-400	**	dry N2

Table 4

BN-1100 & BN-1250
Activation / Stabilization

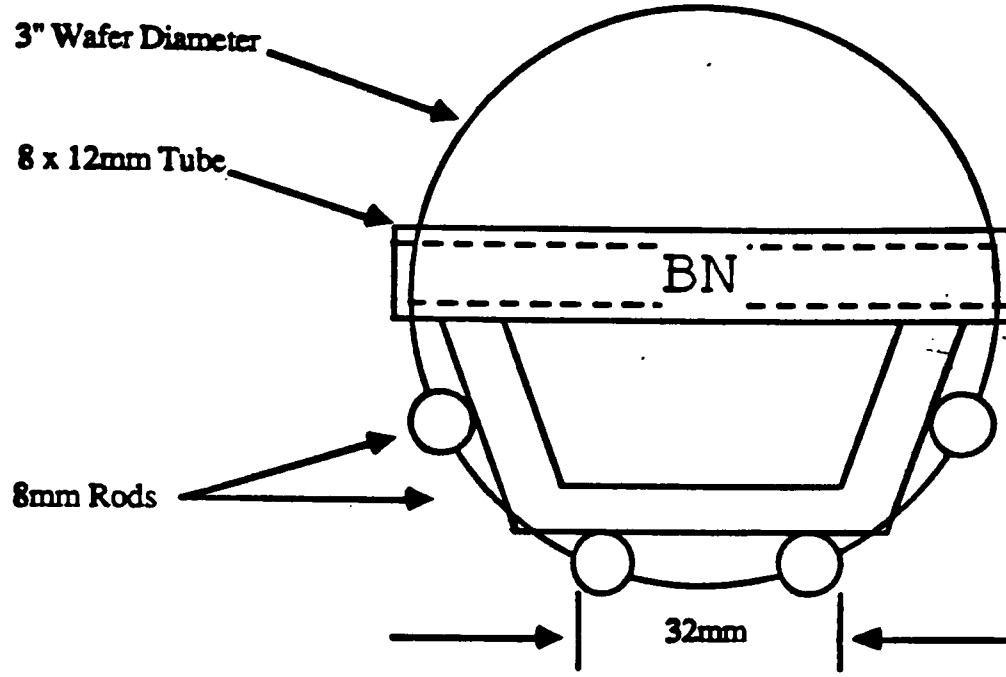
STEP	TEMP (oC)	TIME (min)	GAS
Bake	350-400	60-90	dry N2
Oxidation	1000	30	dry O2
Stabilize	1100 or 1250	1200 (20 hrs)	dry N2
Storage	350-400	**	dry N2

Table 5

The Deposition Cycle

The selection of which boron source is best suited for a specific diffusion process is based on the same criteria used to select a phosphorus source: (1) the target sheet resistance and (2) the temperature at which the diffusion is to take place. Characterization curves, relating sheet resistance to soak time and temperature are use to establish the vital parameters of a deposition process for a desired sheet resistance.

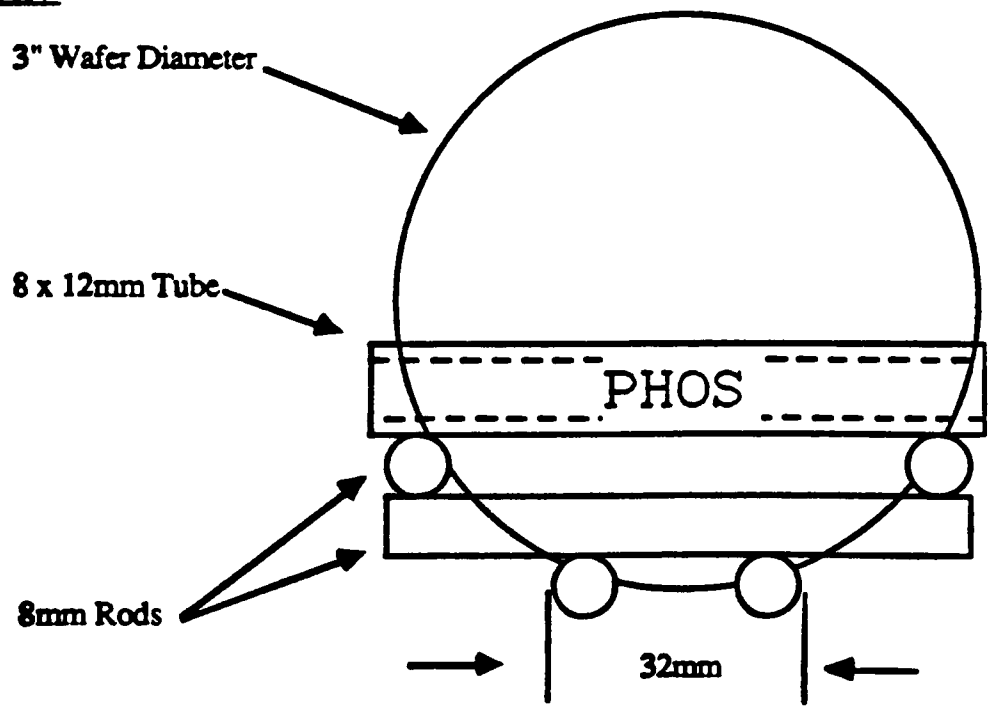
The specialized quartz boat used to hold the boron planar sources and silicon wafers is similar to that used in the deposition of the phosphorus impurity atoms. However, because of the physical difference between the two sources the slot widths in the source boats are different. In order to prevent confusion between the boats their physical designs are also different. The boron source boats are constructed as a medium profile carrier were the phosphorus boats use the low profile design. This is shown in Fig. 2-1a and 2-1b. The basic function of each boat remains unchanged.



BN Medium Profile Carrier

Figure 2-1a

Front View



Phosphorus Low Profile Carrier

Figure 2-1b

Another important difference between the phosphorus and the boron deposition cycles is in the ambient gas flow. Although the total gas flow remains fixed at 5 slpm, the boron deposition cycle uses a 1:1 mixture of nitrogen to oxygen during both the push and pull steps of the cycle. The minute presence of oxygen helps to regenerate the dopant oxide layer both prior to and after the soak step. This procedure helps to prevent the source from becoming depleted after it has been activated. In addition, a flow rate set at 5 slpm serves to block the backflow of contaminants into the diffusion tube and to fill the annular region between the tube wall and the periphery of the wafers. Therefore, dopant transfer from the source wafers occurs in an essentially motionless ambient between the source and semiconductor wafers.

PDS-Boron Nitride
Deposition

STEP	TEMP (oC)	TIME (min)	GAS
Push & Recovery	800	30	N_2:O_2 (5 slpm)
Stabilize	800	15	dry N_2
Ramp-Up	800 - xxx	5 °C/min	dry N_2
Soak	xxx	***	dry N_2
Ramp-Down	xxx - 800	10 °C/min	dry N_2
Pull	800	15	N_2:O_2 (5 slpm)
Storage	600		dry N_2 (2 slpm)

(xxx, *** - predetermined process temperature and time dependent on the desired sheet resistance.)

Table 6

A common problem associated with the use of the boron sources is over oxidation. The build up of excessive amounts B_2O_3 will result in a nonuniform dopant layer on the source wafer. This nonuniform dopant layer will result an uneven transfer of dopant glass to the silicon wafer causing poor sheet resistance uniformity. Stabilizing the source wafers at the process temperature in a non-oxidizing ambient for a period of 1 or 2 hours prior to a deposition will help to alleviate this problem. A stabilization step has also been added to the deposition cycle to assure the dopant oxide layer is uniform after the recovery step has been completed. The periodic reactivation of the sources will become necessary only if the sheet resistance uniformity cannot be controlled through stabilization.

Storing the source wafers correctly is an important step in preventing the excessive build up of dopant oxide. The most effective storing technique is to return the sources to the furnace at a reduce temperature and gas flow of 400°C and 2 slpm respectively. Storing the sources in this manner eliminates the threat of moisture damage caused by humidity changes in the laboratory. If the furnace capacity is not available, storage in an oven or dry box is also acceptable. A dry nitrogen purge should be used with all three of the storage techniques. Prior to reusing the sources each must be stabilized in an non-oxidizing ambient for at least one hour at the process temperature. Extended periods were the wafers are not in use will require a complete reactivation. It is not uncommon to repeat the activation cycle several times in the lifetime of a source.

Process Evaluation

The average glass transfer, the average sheet resistance, and the impurity profile junction depth are the three parameters used in the evaluation of the deposition cycle. The average thickness of the deposited B_2O_3 glass is determined by ellipsometery using a refractive index value of 1.64 [7]. The average sheet resistance of a test wafer can be determined only after the deposited dopant glass is removed. The removal of the dopant glass from the silicon wafers requires a one minute dip in a solution of 10:1 HF. Still present on the wafers will be an unetchable silicon boron complex (Si-B). This complex, typically 200 Å thick, can be removed through a low temperature oxidation (LTO) followed by a second deglaze [6]. The function of the LTO is to rapidly oxidize the Si-B layer and a thin layer of surface silicon allowing minmal dopant diffusion. Table 7 shows an LTO process, run in steam for 15 minutes at 750°C. Empircal studies must be performed in order to determine the optimum LTO cycle necessary to remove the Si-B complex formed during a specific deposition process.

Low Temperature Oxidation
(LTO)

STEP	TEMP (oC)	TIME (min)	GAS
Push	750	15	N_2:O_2 (5 slpm)
Oxidation	750	15	steam
Pull	750	15	N_2:O_2 (5 slpm)
Storage	600	—	dry N_2 (2 slpm)

Table 7

Sheet resistance readings taken prior to the LTO will be lower than readings taken after the Si-B layer is removed. This is due to the fact that the four point probe is measuring the lower resistivity of the Si-B layer in parallel with the diffused layer beneath it. In order qualify a process, sheet resistance measurement taken prior to the LTO are valid in order to determine the amount of resistivity shift that will occur after LTO.

→ The simplest and quickest way to determine the impurity junction is through the grove and stain technique (see Appendix 1). Although this method is destructive it is accurate within ±1% for junctions ≥ one micron [5]. ↖ Appendix B

The collection of this data should be recorded for the specific run and also logged in a record book for lifetime studies of the source. When used correctly any source can last approximately 500 hours of processing time. Indications that a source is depleted will show up in lower glass transfers and higher sheet resistance readings for a standard deposition cycle. Once a source is depleted it is no longer need and can be discarded in a waste bin.

REFERENCES

[1] N. Goldsmith, J. Olmstead, and J. Scott, "Boron Nitride as a Diffusion Source for Silicon", *RCA Review* , June 1967.

[2] S.M. Sze, *VLSI Technology*, chapter 6, McGraw-Hill Book Company, NewYork, 1983.

[3] Kenneth T. Robinson, "PDS Wafers Make It Safe To Dope", *Reasearch and Development*, September 1986.

[4] J. Monkowski and J. Stach, "System Characterization of Planar Source Diffusion", *Solid State Technol.* Nov. 1976.

[5] Carl L. Aley, and R. Scott Turner, "Junction Depth Measuring Methods: The Pros and Cons", *Semicon. Internat.*, May 1980.

[6] Sohio Engineered Materials Company, Product Information, "Low Defect Boron Diffusion Processes Using Hydrogen Injection", Appication Data, Feb. 1986.

[7] *The Merck Index Nineth Edition*, Merck and Co., Inc., Rathway, NJ, 1976.

ROCHESTER INSTITUTE OF TECHNOLOGY
DEPARTMENT OF MICROELECTRONIC ENGINEERING
ESTABLISHING AN N-WELL BIPOLAR FABRICATION SERVICE AT RIT

APPENDIX 3.1

SUPREM III SIMULATIONS

```
**********************************
***        Suprem-III          ***
***   version 1B  rev. 8628    ***
**********************************

    Thu Jun 28 09:27:56 1990


  Commands input from file: fourito.in

 1... Title          RIT N-well Bipolar Electrical Simulation
 2... Comment              Andrew La Pietra
 3... $              file

 4... $              Initialize the silicon substrate.
 5... Initialize     <100> silicon, Boron Concentration=3e15
  ... +              Thickness=10.  dX=.075  XdX=.75 Spaces=100

 6... Comment        Field Oxide for implant
 7... Diffusion      Temperature=1100   Time=25  Wet02

 8... Comment        Etch windows in oxide for implant
 9... Etch           Oxide

10... Comment        Implant and drive-in the Phosphorous layer.
11... Implant        Phosphorous  Dose=8e12  Energy=110
12... Diffusion      Temperature=1150  Time=480  Dry02
13... $Print          Layer
14... $LPPlot         Net Chemical  Xmax=5
15... Diffusion      Temperature=1150  Time=2400
16... Print          Layer
17... LPPlot         Net Chemical  Xmax=15

18... Comment        Etch off the oxide formed during implant
19... Etch           Oxide

20... Comment        Boron Predepostion for base
21... Diffusion      Temperature=800  Time=30  t.rate=5.0  Solidsol Boron

22... $Print          Layer

23... Comment        Boron Predepostion for base
24... Diffusion      Temperature=950  Time=10  t.rate=0.0  Boron  Solidsol

25... Comment        Boron Predepostion for base
26... Diffusion      Temperature=950  Time=30  t.rate=-5.0  Boron  solidsol
27... $Print          Layer
28... $LPplot         Net Chemical Xmax=9

29... Comment        This is the LTO step to reduce base diffusion damage
30... Diffusion      Temperature=750  Time=25 Wet02

31... Comment        Removal of BSG
32... Etch           Oxide

33... Comment        Boron Drive-in plus field oxidation for phos. diff
34... Diffusion      Temperature=1100  Time=30  Wet02
35... Diffusion      Temperature=1150  Time=20  Dry02

36... Comment        Oxide removal for rework
37... Etch           Oxide

38... Comment        Phos. Predepostion for emitter
39... Diffusion      Temperature=800  Time=35  t.rate=5.0 phosphor solidsol

40... Comment        Phos. Predepostion for emitter
41... Diffusion      Temperature=975  Time=20  t.rate=0.0  phosphor solidsol

42... Comment        Phos. Predepostion for emitter
43... Diffusion      Temperature=975  Time=35  t.rate=-5.0 phosphor solidsol
44... $Print          Layer
45... $LPplot         Net Chemical Xmax=15

46... Comment        Removal of PSG
47... Etch           Oxide

48... Comment        Phos. drive-in and CC mask
49... Diffusion      Temperature=1050  Time=20  Wet02

50... Comment        CC opening
51... Etch

52... Print          Layer
53... LPplot         Net Chemical Xmax=10

54... Savefile       Structure File=fourelec.in
55... Stop
```

layer no.	material type	thickness (microns)	dx (microns)	dxmin	top node	bottom node	orientation or grain size
1	SILICON	9.2806	0.0750	0.0010	409	500	<100>

Integrated Dopant

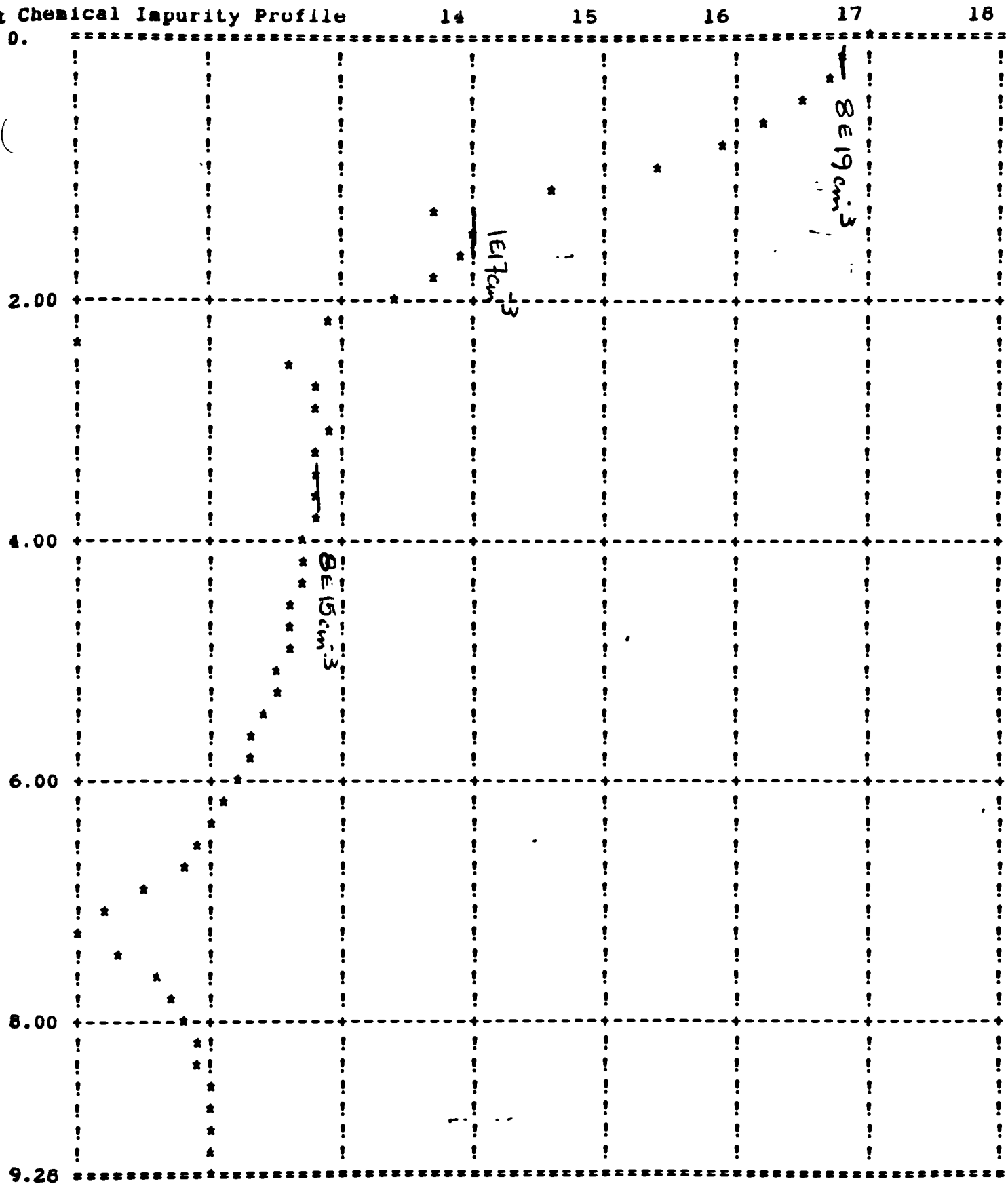
layer no.	Net active	Net chemical	Total active	Total chemical
1	3.6159e+15	3.8371e+15	3.7639e+15	3.9851e+15
sum	3.6159e+15	3.8371e+15	3.7639e+15	3.9851e+15

Integrated Dopant

layer no.	BORON active	BORON chemical	PHOSPHORUS active	PHOSPHORUS chemical
1	7.3982e+13	7.3982e+13	3.6899e+15	3.9111e+15
sum	7.3982e+13	7.3982e+13	3.6899e+15	3.9111e+15

Junction Depths and Integrated Dopant Concentrations for Each Diffused Region

layer no.	region no.	type	junction depth (microns)	net active Qd	total chemical Qd
1	4	n	0.	3.6201e+15	3.9637e+15
1	3	p	1.4151	5.8464e+12	1.1481e+13
1	2	n	2.5784	1.7227e+12	4.6577e+12
1	1	p	7.2790	1.4160e+11	1.0445e+12


t Chemical Impurity Profile
14
15
16
17
18
0.
2.00
4.00
6.00
8.00
9.26
8E19 cm-3
1E17cm-3
8E15cm-3

Suprem-III

```
**********************************
***        Suprem-III          ***
***   version 1B  rev. 8628    ***
**********************************

    Tue Jul  3 09:48:14 1990


  Commands input from file: fourelel.in

 1... Title           RIT N-well Bipolar Electrical Simulation
 2... Comment               Andrew La Pietra
 3... $               This is for fourth.out simulation

 4... Initialize      Structure=fourelec.in
 5... Comment         This is where the physical structure is stored

 6... Comment         Solve Poisson's equation with the collector ramped
 7... $               from 0 to 20 volts in 2 volt steps

 8... Electrical      Extent=8 Steps=10 file.out=fourelec.out
 9... Bias            Layer=1 Diffusion=3 V.Minority=0 DV.Minority=2
10... Bias            Layer=1 Diffusion=2 V.Majority=0 DV.Majority=2
11... Bias            Layer=1 Diffusion=1 V.Minority=0 DV.Minority=2
12... End
13... $
14... Comment         Plot impurity profile
15... Plot            Active Net Total
16... Stop


RIT N-well Bipolar Electrical Simulation
Andrew La Pietra
This is for fourth.out simulation

This is where the physical structure is stored
Solve Poisson's equation with the collector ramped
from 0 to 20 volts in 2 volt steps

Required Iterations =  5

0V

Step Layer Region     Concentration          Conductivity          Sheet
                      Holes      Electrons   Holes      Electrons  Resistivity
  1    1      4   0.000e+00  3.066e+15  0.000e+00  3.571e+02  2.438e+01
  1    1      3   2.776e+13  5.095e+03  7.296e+00  5.032e-09  1.025e+03
  1    1      2   1.726e+04  4.512e+12  2.410e-09  1.450e+00  1.295e+03
  1    1      1   7.750e+11  1.653e+05  1.402e-01  2.580e-07  1.707e+04

Required Iterations =  8

Step Layer Region     Concentration          Conductivity          Sheet
                      Holes      Electrons   Holes      Electrons  Resistivity
  2    1      4   0.000e+00  3.066e+15  0.000e+00  3.571e+02  2.438e+01
  2    1      3   2.752e+13  0.000e+00  7.193e+00  0.000e+00  1.039e+03
  2    1      2   0.000e+00  4.194e+12  0.000e+00  1.355e+00  1.386e+03
  2    1      1   7.110e+11  0.000e+00  1.048e-01  0.000e+00  1.856e+04

Required Iterations =  10

Step Layer Region     Concentration          Conductivity          Sheet
                      Holes      Electrons   Holes      Electrons  Resistivity
  3    1      4   0.000e+00  3.066e+15  0.000e+00  3.571e+02  2.438e+01
  3    1      3   2.734e+13  0.000e+00  7.122e+00  0.000e+00  1.050e+03
  3    1      2   0.000e+00  3.968e+12  0.000e+00  1.287e+00  1.460e+03
  3    1      1   6.665e+11  0.000e+00  3.795e-01  0.000e+00  1.980e+04

Required Iterations =  10

Step Layer Region     Concentration          Conductivity          Sheet
                      Holes      Electrons   Holes      Electrons  Resistivity
  4    1      4   0.000e+00  3.066e+15  0.000e+00  3.571e+02  2.438e+01
  4    1      3   2.718e+13  0.000e+00  7.060e+00  0.000e+00  1.059e+03
  4    1      2   0.000e+00  3.774e+12  0.000e+00  1.227e+00  1.531e+03
  4    1      1   6.297e+11  0.000e+00  3.585e-01  0.000e+00  2.096e+04

Required Iterations =  11

Step Layer Region     Concentration          Conductivity          Sheet
                      Holes      Electrons   Holes      Electrons  Resistivity
  5    1      4   0.000e+00  3.066e+15  0.000e+00  3.571e+02  2.438e+01
  5    1      3   2.704e+13  0.000e+00  7.005e+00  0.000e+00  1.067e+03
  5    1      2   0.000e+00  3.599e+12  0.000e+00  1.173e+00  1.601e+03
  5    1      1   5.974e+11  0.000e+00  3.401e-01  0.000e+00  2.209e+04

Required Iterations =  11

10V

Step Layer Region     Concentration          Conductivity          Sheet
                      Holes      Electrons   Holes      Electrons  Resistivity
  6    1      4   0.000e+00  3.066e+15  0.000e+00  3.571e+02  2.438e+01
  6    1      3   2.692e+13  0.000e+00  6.958e+00  0.000e+00  1.074e+03
  6    1      2   0.000e+00  3.446e+12  0.000e+00  1.125e+00  1.669e+03
  6    1      1   5.662e+11  0.000e+00  3.235e-01  0.000e+00  2.322e+04

Required Iterations =  12
```

ROCHESTER INSTITUTE OF TECHNOLOGY
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ESTABLISHING AN N-WELL BIPOLAR FABRICATION SERVICE AT RIT

APPENDIX 4.1

RIT BIPOLAR FABRICATION SERVICE

USERS DESIGN MANUAL

ROCHESTER INSTITUTE OF TECHNOLOGY

DEPARTMENT OF MICROELECTRONIC ENGINEERING

BIPOLAR INTEGRATED CIRCUIT DESIGN MANUAL FOR THE RIT N-WELL BIPOLAR FABRICATION SERVICE

Location: Microlib account, Analog directory
Document: Manuall.rno
Revision Date: 1/15/91

ROCHESTER INSTITUTE OF TECHNOLOGY
DEPARTMENT OF MICROELECTRONIC ENGINEERING
N-WELL BIPOLAR INTEGRATED CIRCUIT DESIGN MANUAL

TABLE OF CONTENTS

ROCHESTER INSTITUTE OF TECHNOLOGY
DEPARTMENT OF MICROELECTRONIC ENGINEERING
N-WELL BIPOLAR INTEGRATED CIRCUIT DESIGN MANUAL

INTRODUCTION

This manual is for students and faculty interested in designing analog integrated circuits with the intention of obtaining fabricated chips from the Microelectronic Engineering department. Designs are fabricated using a triple diffusion process that electrically isolates circuitry with an implanted n-type well. The result is a bipolar process that is not capable of high current output, but otherwise is a complete proess.

The circuitry is implemented into layout form using ICE. ICE, which stands for Integrated Circuit Editor, is a CAD tool with the basic function of drawing boxes and saving the locations in CALTECH Intermediate Format, or CIF. Several different colors are used in ICE with each color representing a different fabrication mask level. ICE knows which colors are assigned to specific levels and other information such as design area by reading a process file at the beginning of each ICE session. The RIT N-Well bipolar fabrication service uses a five level process, and the levels are defined as Nwell, base, emitter, cc (for contact cut) and metal. A buried layer is also available for use with an epitaxial process. ICE is VAX resident so it provides campus wide accessibility for students and faculty using a VT240 or higher terminal. ICE can also be accessed via modem by using a VT240 or higher software emulator.

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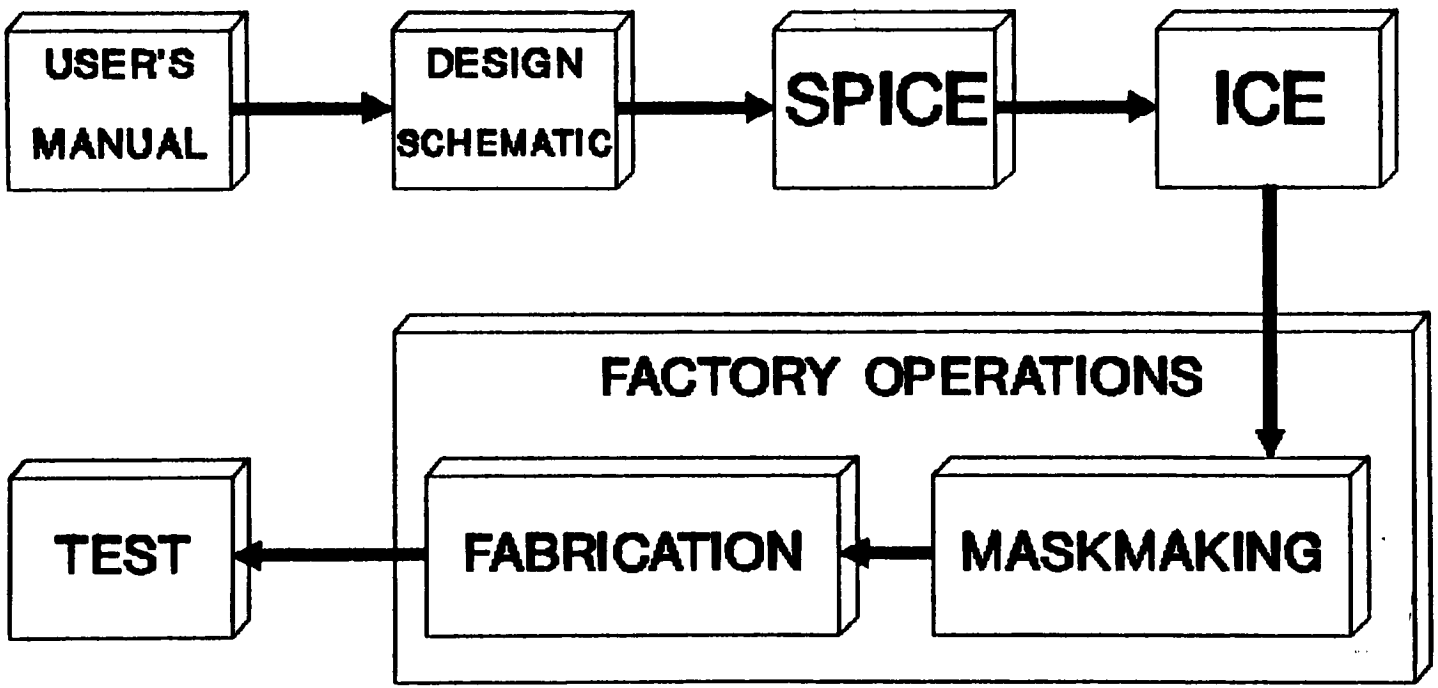
N-WELL BIPOLAR INTEGRATED CIRCUIT DESIGN MANUAL

PROCESS OVERVIEW

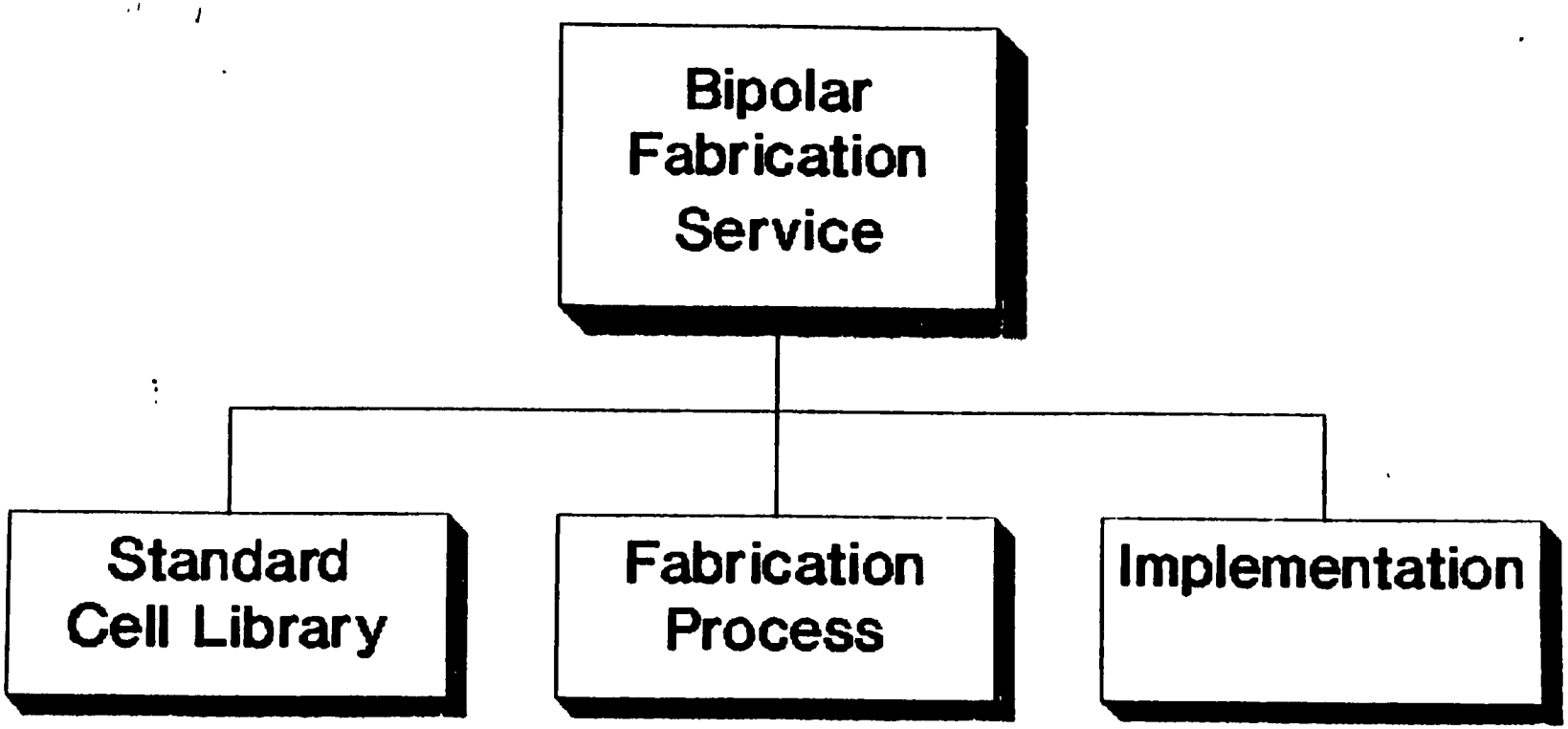
OF

RIT N-WELL BIPOLAR PROCESS

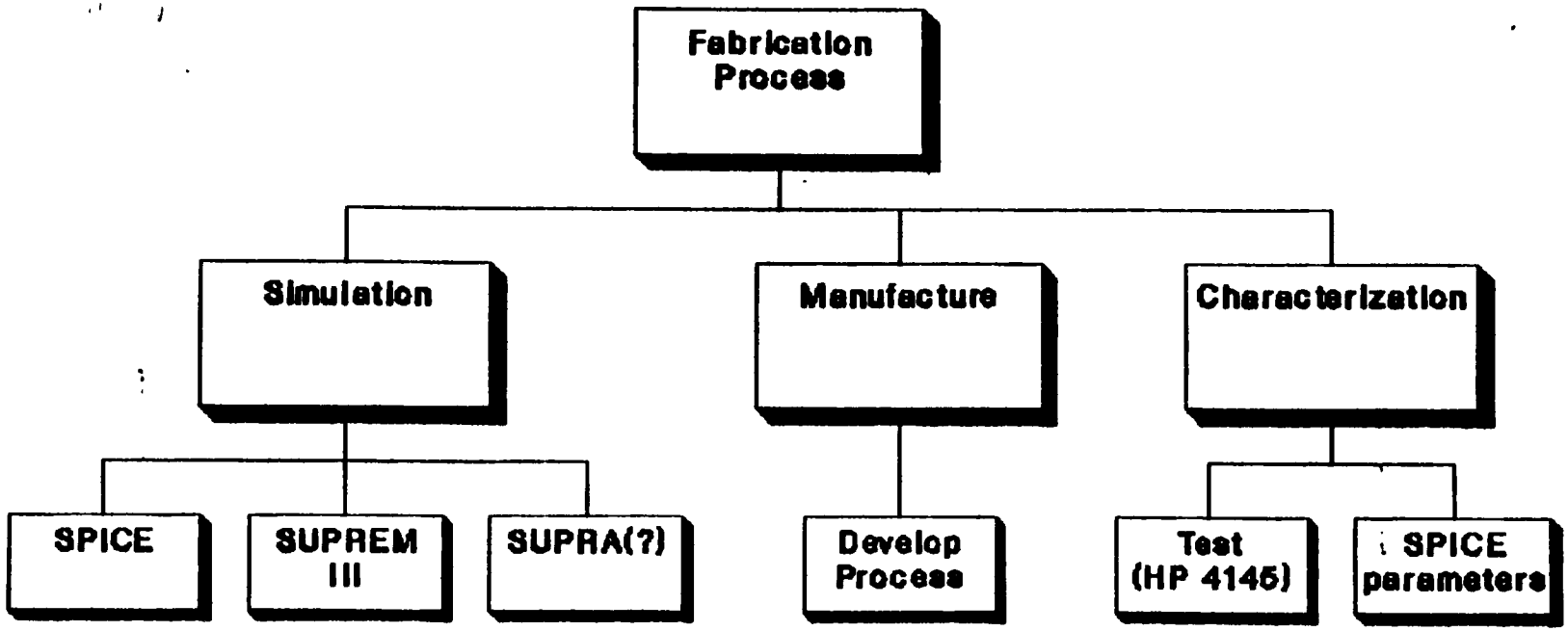
RIT N-WELL BIPOLAR SERVICE
FABRICATION SEQUENCE

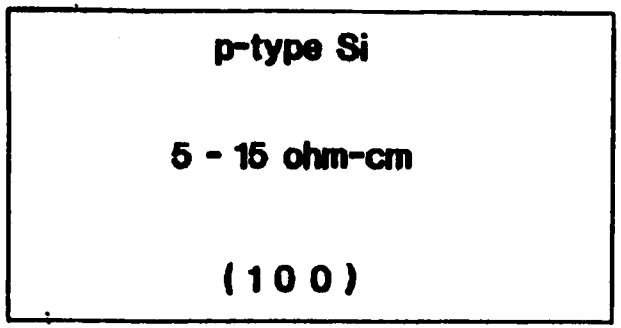


RIT N-Well Bipolar Fabrication Service



RIT N-Well Bipolar Fabrication Service

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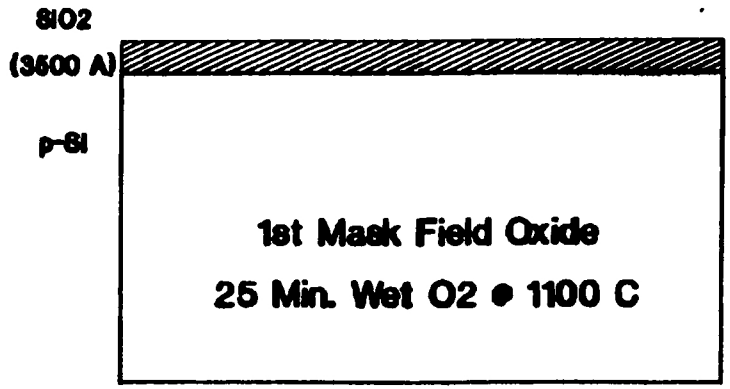
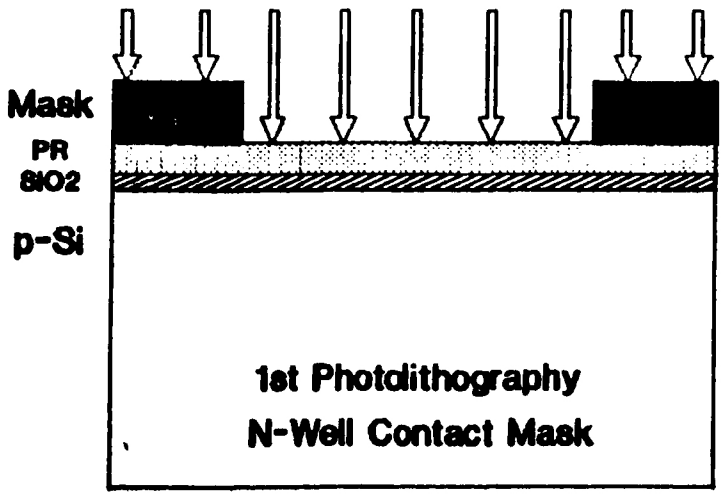
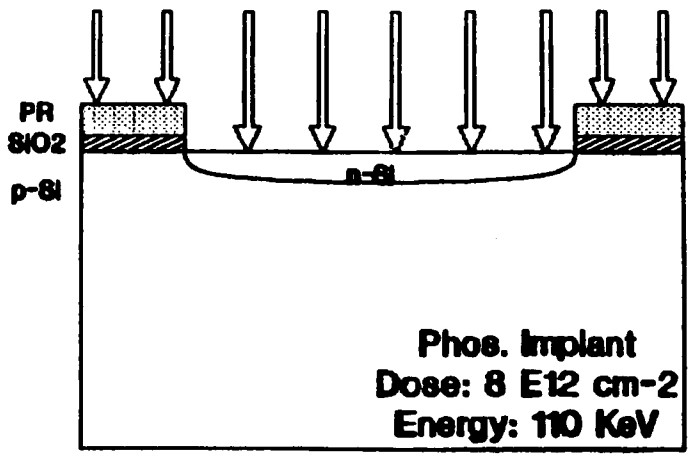
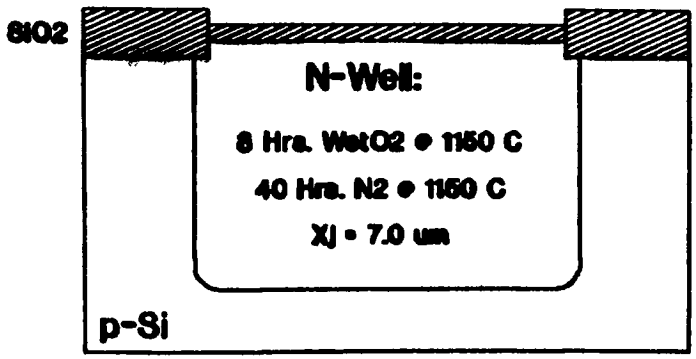
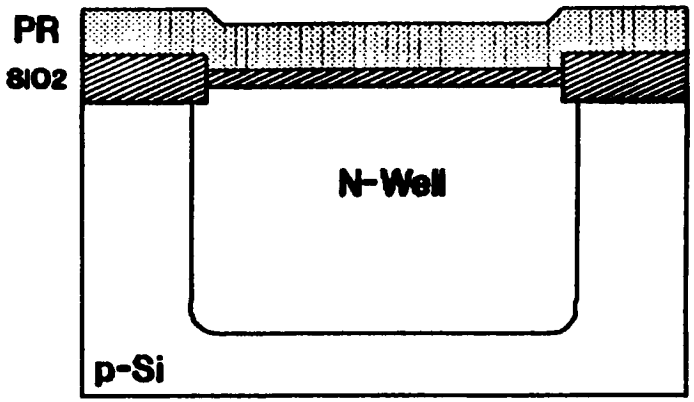
5 - 15 ohm-cm
(1 0 0)

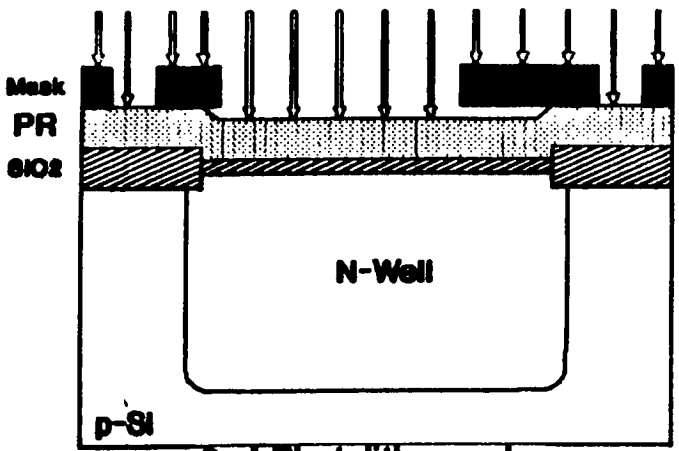

SiO2
(3500 A)
p-Si
1st Mask Field Oxide
25 Min. Wet O2 @ 1100 C


Mask
PR
SiO2
p-Si
1st Photolithography
N-Well Contact Mask

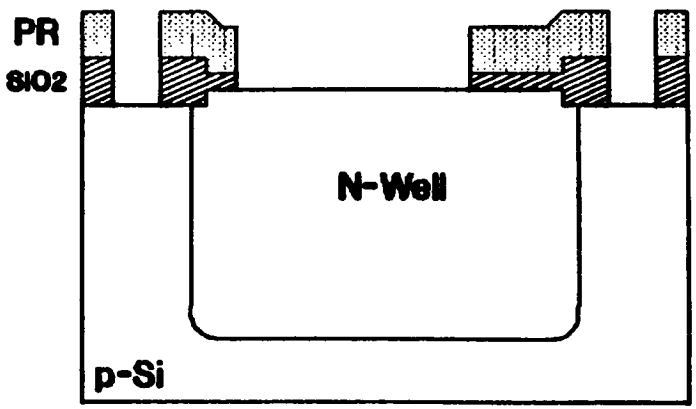

PR
SiO2
p-Si
n-Si
Phos. Implant
Dose: 8 E12 cm-2
Energy: 110 KeV



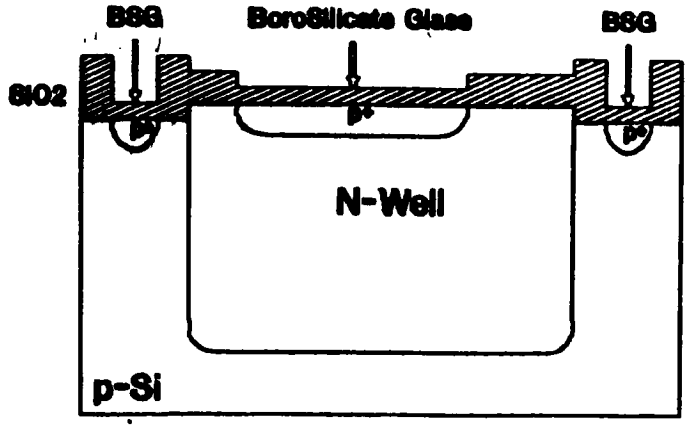




2nd Photolithography
Base Deposition Contact Mask

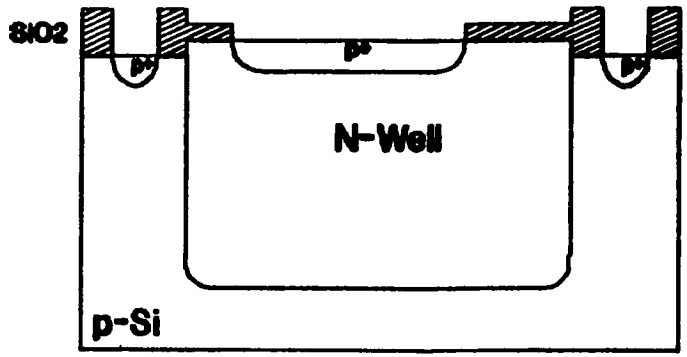


Opening Base Diffusion Windows

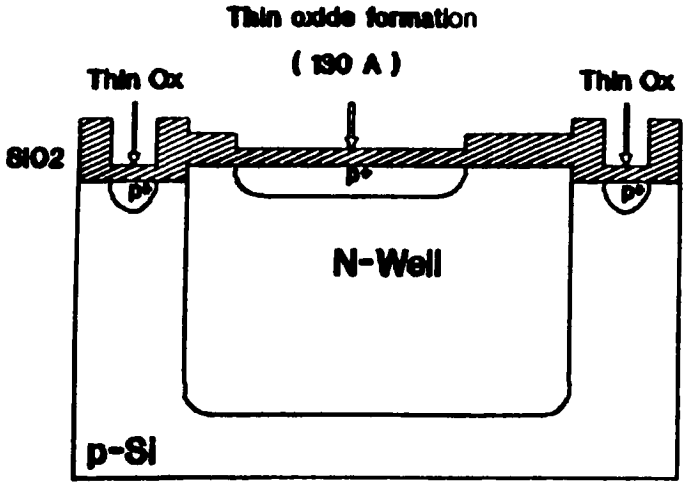


Boron Solid Diffusion Source Predeposition

10 Minutes @ 950 C

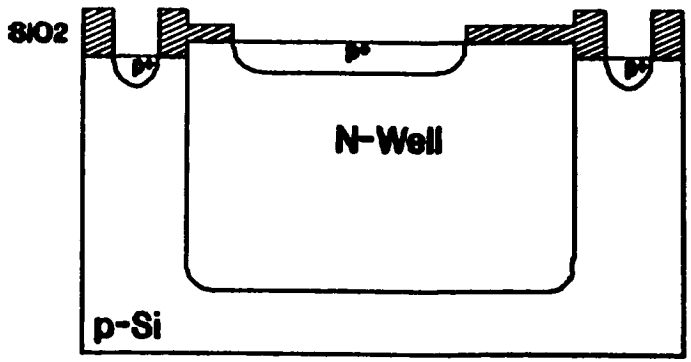


Etch Back BSG

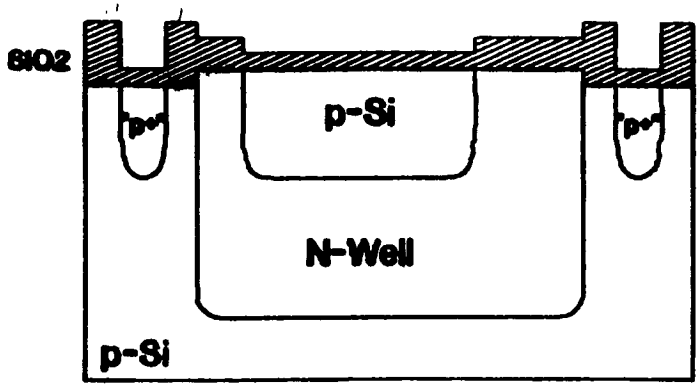


Low Temperature Oxide to reduce deposition damage

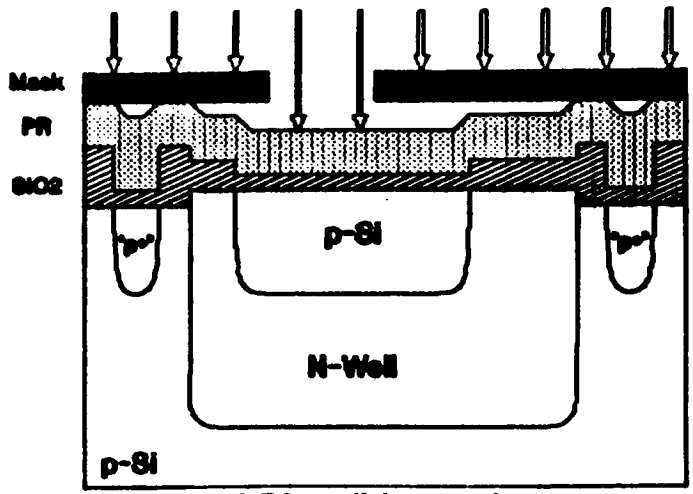
25 Minutes @ 750 C Wet O2



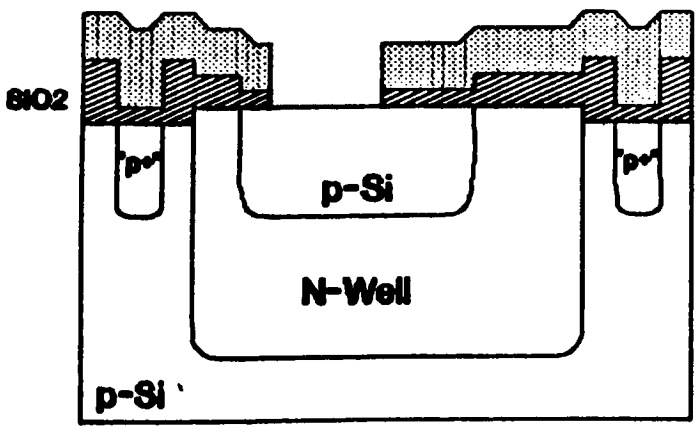
Etch Back LTO to remove trapped damage



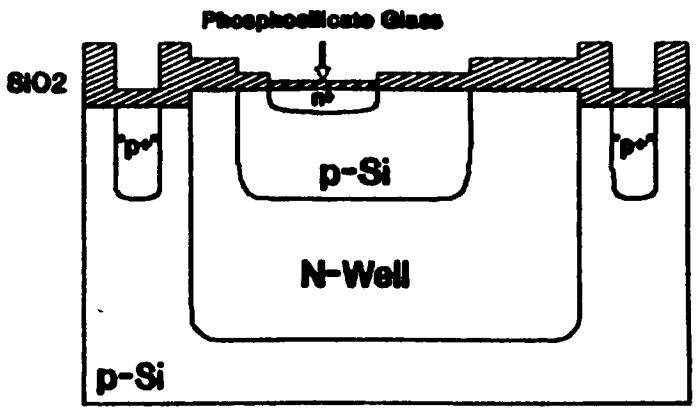
Base Drive-in: 30 Min. Wet O2 @ 1100 C
20 Min. Dry O2 @ 1150 C



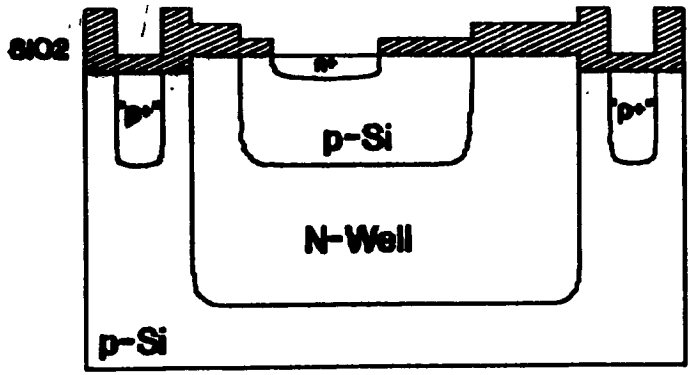
3rd Photolithography
Emitter Contact Mask



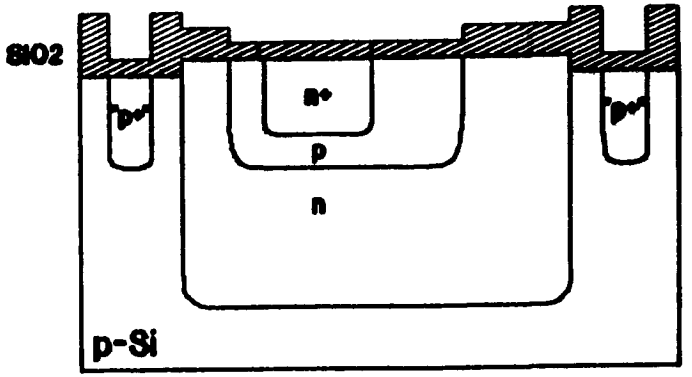
Open Emitter Diffusion Windows



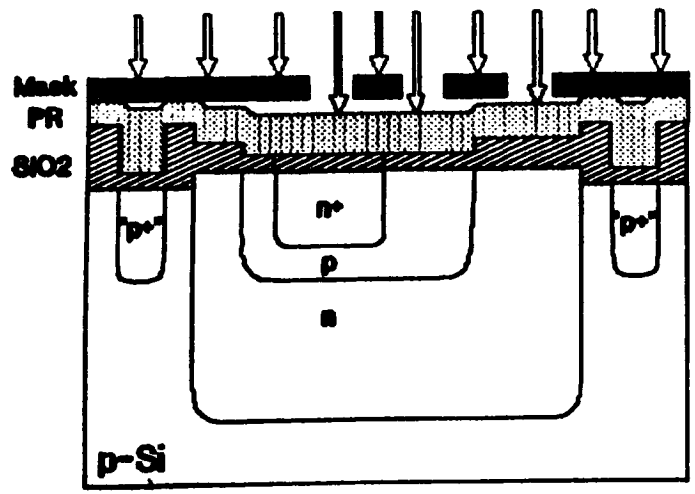
Emitter Predeposition: Phosphorous Solid Source
10 Minutes @ 975 C



Etch Back Phoephosilicate Glass

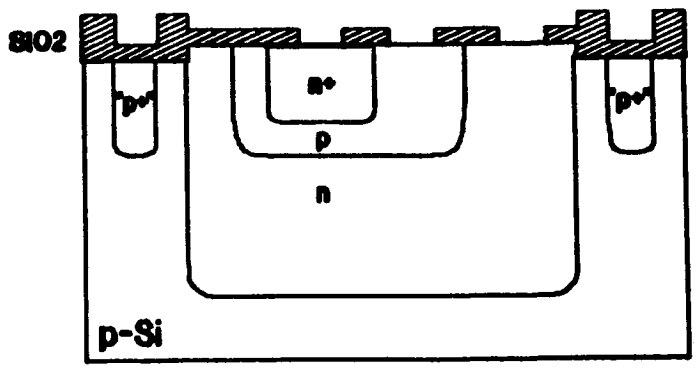


Emitter Drive-in: 15 Min. @ 1100 C Wet O2

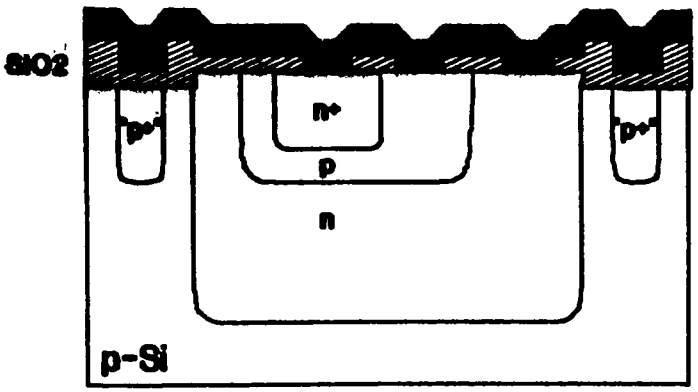


4th Photolithography

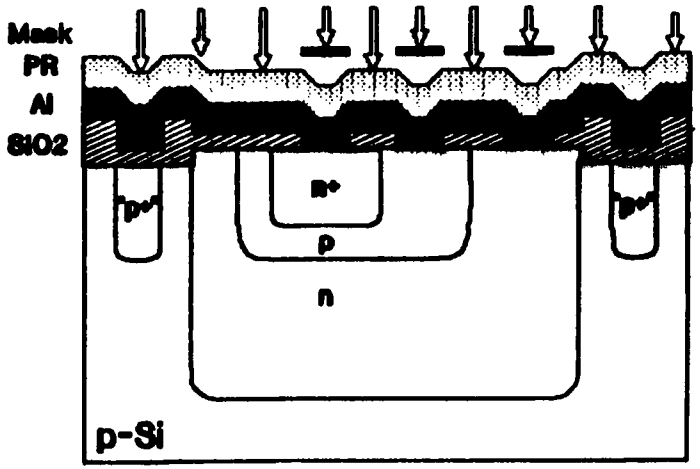
Contact Cut Mask



Contact Cut Formation

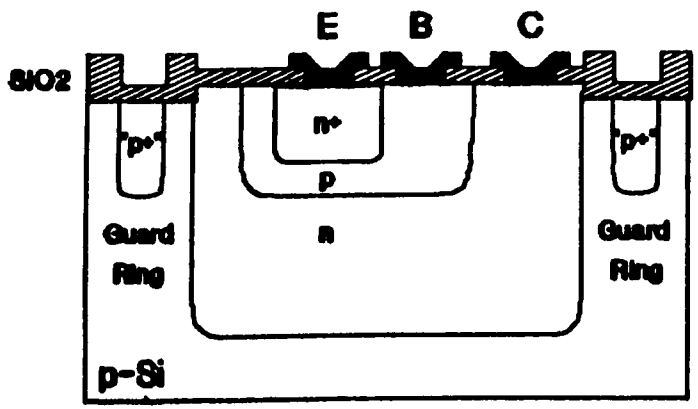


Aluminum Deposition

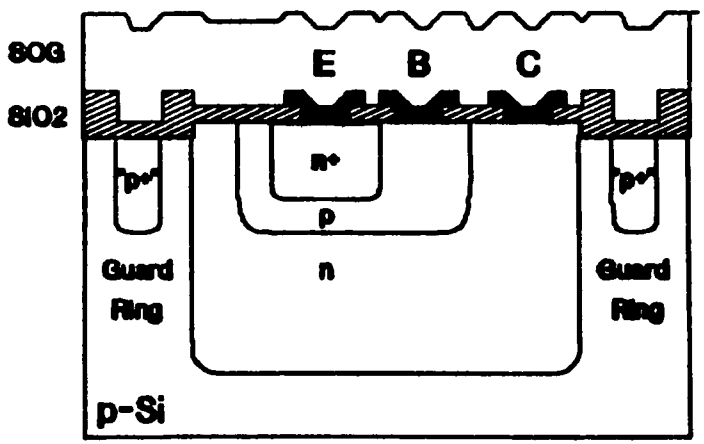


5th Photolithography

Metal Mask

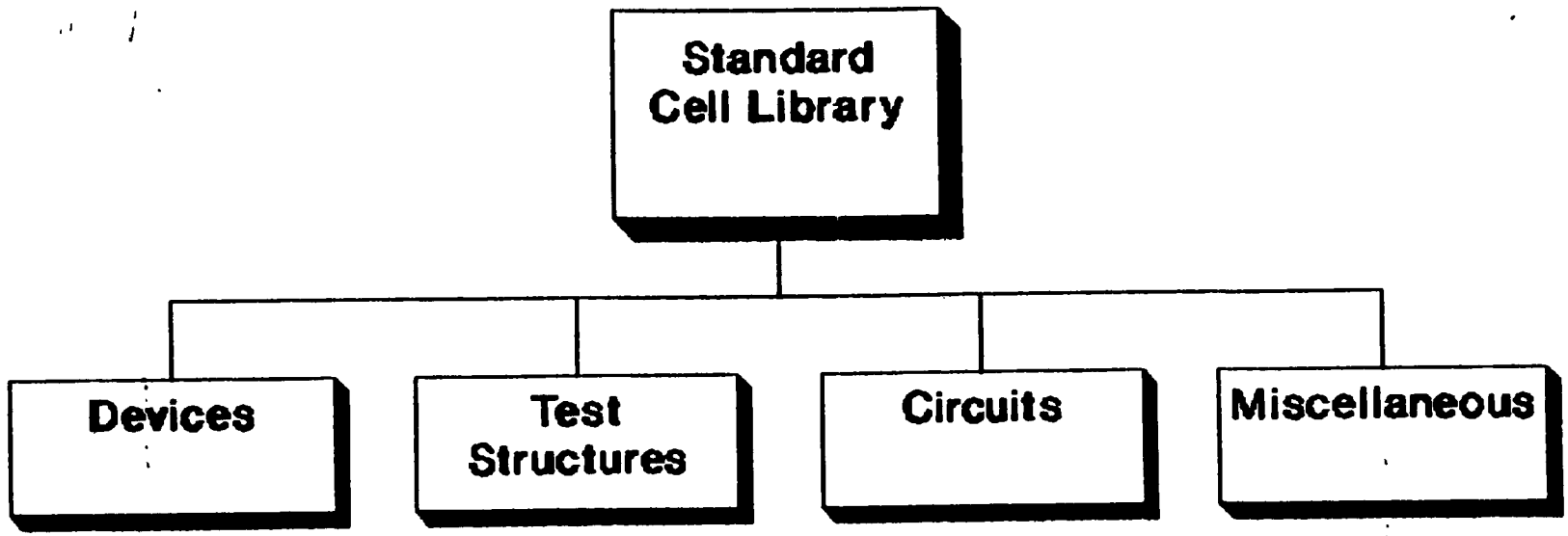


Final NPN Structure

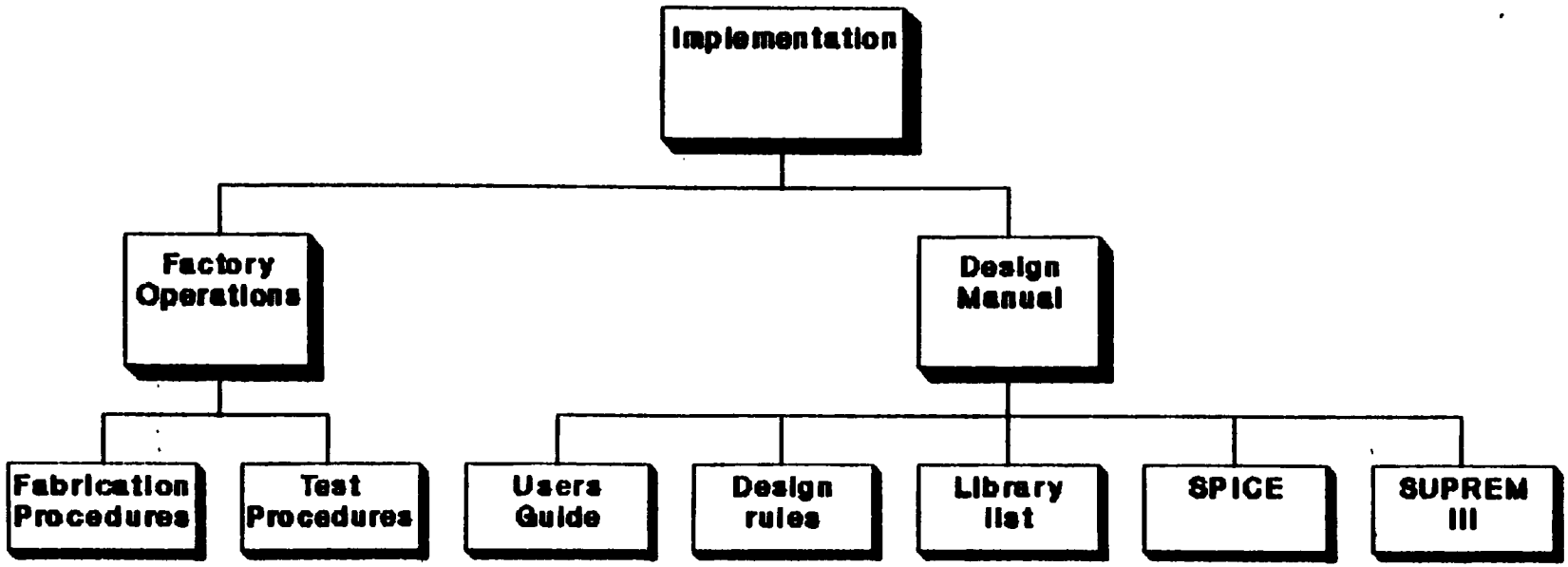


Spin-on-Glass Passivation layer
(to reduce surface leakage)

RIT N-Well Bipolar Fabrication Service



RIT N-Well Bipolar Fabrication Service



RIT N-Well Bipolar Fabrication Service

Lambda Based Design Rules

10 Micron minimum geometry design rules are used for this process since the high voltages (5 volts or greater) can cause electrically isolated regions to short via reverse bias depletion region extension. (Lambda = L = 10 Microns)

Wc = L ; CONTACT CUT WIDTH (MIN.)
Wb = L ; BASE DIFFUSION WIDTH (MIN.)
We = L ; EMITTER DIFFUSION WIDTH (MIN.)
Wm = L ; METAL WIDTH (MIN.)

Ebc = L ; BASE EXTENSION BEYOND CONTACT CUT (MIN.)
Eec = L ; EMITTER EXTENSION BEYOND CONTACT CUT (MIN.)
Emc = L ; METAL EXTENSION BEYOND CONTACT CUT (MIN.)
Ewb = L ; N-WELL EXTENSION BEYOND BASE (MIN.)
Ebe = L ; BASE EXTENSION BEYOND EMITTER (MIN.)
Eeb = L ; EMITTER EXTENSION BEYOND BASE FOR PINCH RESISTORS (MIN.)

Smm = L ; ADJACENT METAL REGION SPACING (MIN.)
Sww = L ; ADJACENT N-WELL REGION SPACING (MIN.)
Sbb = 2L ; ADJACENT BASE REGION SPACING (MIN.)
Sgw = L ; N-WELL & GUARD RING SPACING (MIN.)

Rules created by Dr. Lynn Fuller (ARL 7/12/90)

ROCHESTER INSTITUTE OF TECHNOLOGY - MICROELECTRONIC ENGINEERING
N-WELL BIPOLAR INTEGRATED CIRCUIT DESIGN MANUAL

LAYOUT GUIDELINES

1.0 The chip size is 4000 by 4000 micrometers. A 250 micrometer region along the left side and 300 micrometer along the bottom are reserved for alignment marks, resolution targets, test structures, etc. leaving 3750 by 3700 micrometer region for the designer.

2.0 When using ICE only use layer names given in the process file, NWELL_BIPOLAR.ICE That is : METAL, EMITTER, NWELL, BASE, and CC. To get a copy of this file into your account type COPY USER7:[MICROLIB.ICE.BIPOLAR]NWELL_BIPOLAR.ICE *.*;*

3.0 Since the n-well diffusion is very deep (8-10 micrometers) and lateral diffusion is approximately the same, adjacent n-well regions should be separated by 30 micrometers.

4.0 To minimize the number of n-well regions it is possible to place diffused base resistors in the same n-well; Transistors with collectors connected together can go in the same n-well.

5.0 An n+ and metal contact must be made to each n-well and connected to a positive voltage with respect to the substrate to keep the n-well substrate junction reverse biased.

6.0 Several substrate contacts should be provided to connect the p-type substrate to the most negative supply voltage.

7.0 Aluminum bonding pads should be 100X100 micrometer. A standard pad location is recommended so that the probe cards already available can be used. (See cell library)

8.0 Each n-well should be surrounded by a diffused p-type guard ring (the base diffusion). This p-type diffusion can be as small as 10 micrometer wide located in the center of the 30 micrometer wide space between n-wells. This ensures that the wafer surface has enough boron to prevent depletion during oxide growth and possible inversion.

9.0 Emitter diffused crossunders can be used. Supply lines should be metal not diffusion. If they must crossunder make a short wide crossunder.

10.0 Diffused base resistors can be a minimum of 10 micrometers wide, however the width is comparable to the lateral diffusion (and junction depth) of about 3 micrometers on each side and therefore the side wall conductance is significant. Sheet resistances given by wide structures, four point probe or Van der Paw techniques do not account for the sidewall conductances.

$$R = 1/(2*(GsideL/L) + W/Rhos*L) + 2*Rc + 2*Rt$$

where Rc is the aluminum to silicon contact resistance of

about 1.24E-4 mho/um2

Rt is the termination resistance of about 0.65*Rhos for W x W, 3W x 3W design.

Rhos is the sheet resistance from four point probe

L is the resistor length

W is the resistor width

GsideL is the sidewall conductance per unit length and is calculated knowing the diffusion profile (try 0.1 mho micrometers if profile is not known)

Example: Given Rhos=35 ohm, W=10 um, find L for a 3000 ohm resistor.

3000 = L/(2*(0.1)+10/35) + 2/(10*10*1.24e-4) +2*.65*35

3000 = L/.486 + 161 + 45.5

L = 1358 micrometers

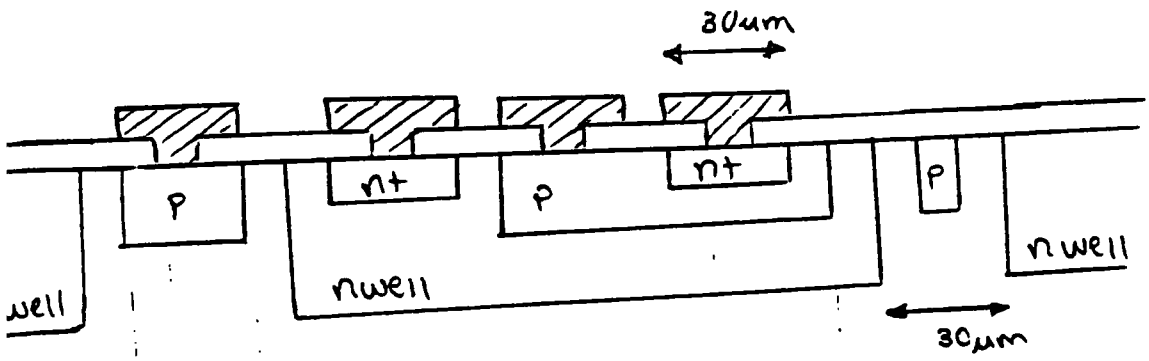
11.0 Use letters to create labels for VIN, VOUT, VDD, VEE, GND etc. A set of letters can be obtained from the cell library.

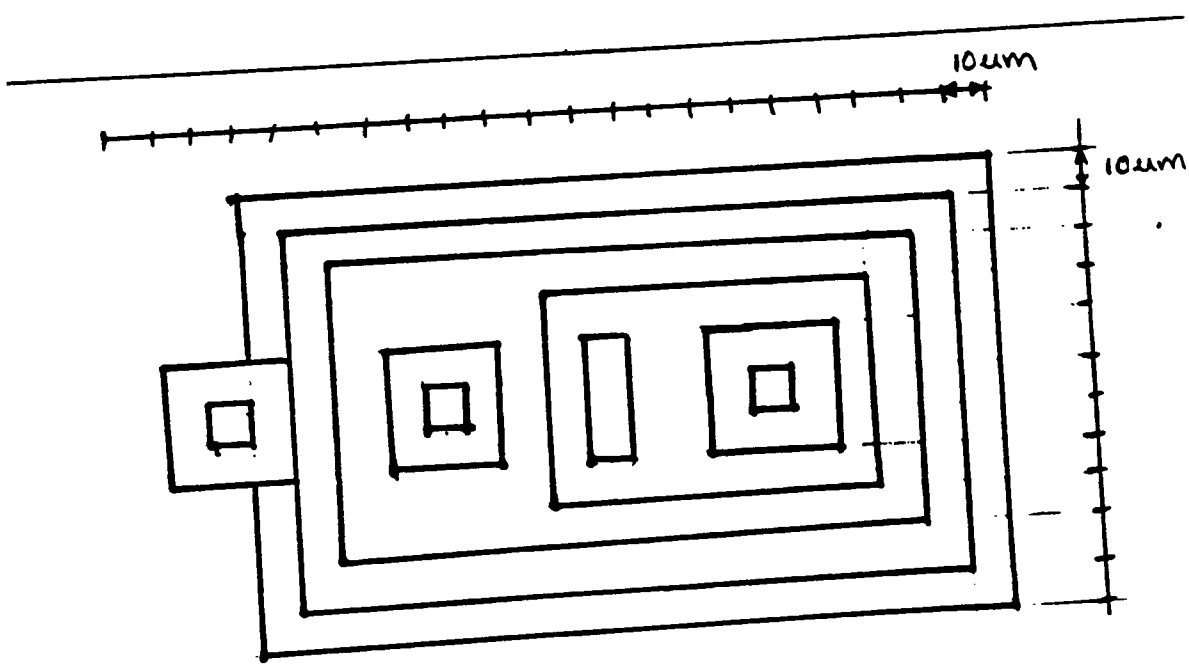
12.0 Resolution targets, alignment marks and test structures need to be included and can be obtained from the cell library.

13.0 Mann files need to be generated and these are electronically mailed to the factory for maskmaking.

14.0 Plot files can be made and plots of the circuit made for checking.

SAMPLE NPN TRANSISTOR LAYOUT





ICE; GETTING STARTED

ICE is a computer program that was written by Taylor Hogan for use by integrated circuit designers at RIT. The program allows the creation and editing of integrated circuits. It is limited to 16 layers and to rectangular boxes and traces. It is easy to learn and is available on any graphics terminal connected to the RIT VAX system by typing the command ICE. In addition ICE will generate the files needed to run the pattern generator which is the first step in maskmaking in the RIT integrated circuit laboratory.

Procedure:

1.0 Log onto your account from a graphics terminal (VT240,VT340)
2.0 Create a subdirectory to keep your ICE design files together.
3.0 Copy process file: NWELL_BIPOLAR.ICE
Copy cell library: NWELL*.CIF
Copy color set up: ICECOLORS.COM
Copy letters : Z*.CIF
4.0 Type TYPE ICECOLORS.COM to set up colors for a VT240 or VT340
5.0 Type ICE
6.0 Type NWELL_BIPOLAR.ICE
7.0 Type GIGI
8.0 Use ice commands such as LAYER BASE
BOX
ZOOM
BOX

```
RIT_BIPOLAR_5_LEVEL_PROCESS_NWELL_BIPOLAR.ICE
chip width = 4000 chip height = 4000
7 layers
layer metal 0 anti regions
plot 1 graphics 1

layer emitter 1 anti regions
0 300 250 1700
plot 2 graphics 2

layer nwell 1 anti regions
0 300 250 1700
plot 3 graphics 3

layer base 1 anti regions
0 300 250 1700
plot 4 graphics 4

layer extra 0 anti regions
plot 5 graphics 5

layer buried 0 anti regions
plot 6 graphics 6

layer cc 1 anti regions
0 300 250 1700
plot 7 graphics 7

1  color 1 pen 3 fill 0 angle 0 space 1
2  color 2 pen 2 fill 0 angle 0 space 1
   color 3 pen 3 fill 0 angle 0 space 1
4  color 4 pen 4 fill 0 angle 0 space 1
5  color 5 pen 5 fill 0 angle 0 space 1
6  color 6 pen 6 fill 0 angle 0 space 1
7  color 7 pen 1 fill 0 angle 0 space 1
8  color 8 pen 8 fill 0 angle 0 space 1
9  color 1 pen 1 fill 0 angle 0 space 1
10 color 2 pen 2 fill 0 angle 0 space 1
11 color 3 pen 3 fill 0 angle 0 space 1
12 color 4 pen 4 fill 0 angle 0 space 1
13 color 5 pen 5 fill 0 angle 0 space 1
14 color 6 pen 6 fill 0 angle 0 space 1
15 color 7 pen 7 fill 0 angle 0 space 1
16 color 8 pen 8 fill 0 angle 0 space 1
```

ICE REFERENCE SHEET

To begin, run the ICECOLORS.COM program and type ICE at the VAX prompt

```
$ @ICECOLORS
$ ICE
```

It will return with ENTER PROCESS FILENAME:

Enter XXX.ICE where XXX corresponds to a particular fabrication process

It will return with ICE> prompt. Type GIGI at the prompt.

LOGICAL COMMANDS

BOX <layer name> - Used to draw a box on a given level. Defaults to presently defined layer
CLONE - Copies the last selected or grouped symbol. Hit return twice to discontinue.
DELETE - Removes the last selected or grouped symbol.
GROUP - Forms one symbol from selected objects.
LAYER <layer name> - Defines which level is being used
MOVE - Moves a selected object to a desired location
MX or MY - Mirrors selected object about X or Y axis
SELECT <layer names> - Used to pick-up an one or several objects. If Layer names are specified it will only pick-up items from those layers. Defaults to selecting items on all layers.
TRACE [width] - Used to make a standard width box on defined layer.

SCREEN COMMANDS

REDRAW - Refreshes screen
RESET - Returns drawing to original size
SHOW <Layer name> - Shows specified layers on screen. SHOW ? shows all layers.
SYMDISP - Displays current selected symbol in lower right blue box.
ZOOM <scale factor> - Magnifies or demagnifies screen. The scale factor must be and integer and defaults to +2 (2 times size).

FILE MANAGEMENT

SYMIN [filename] - Brings a previously designed symbol into design space. The symbol can be positioned as desired.
PROJIN [fn] - Brings design into design space as designed.

SYMOUT [fn] - Saves the last ^&SELECTED\& objects and places them into a .CIF file. Remember to select the WHOLE design space to save the design.
PROJOUT [fn] - Saves whatever is in current design space

POST PROCESSORS

PLOT [fn] - creates HP plotter file on all design levels. Make sure that the plotter is set to give proper scaling

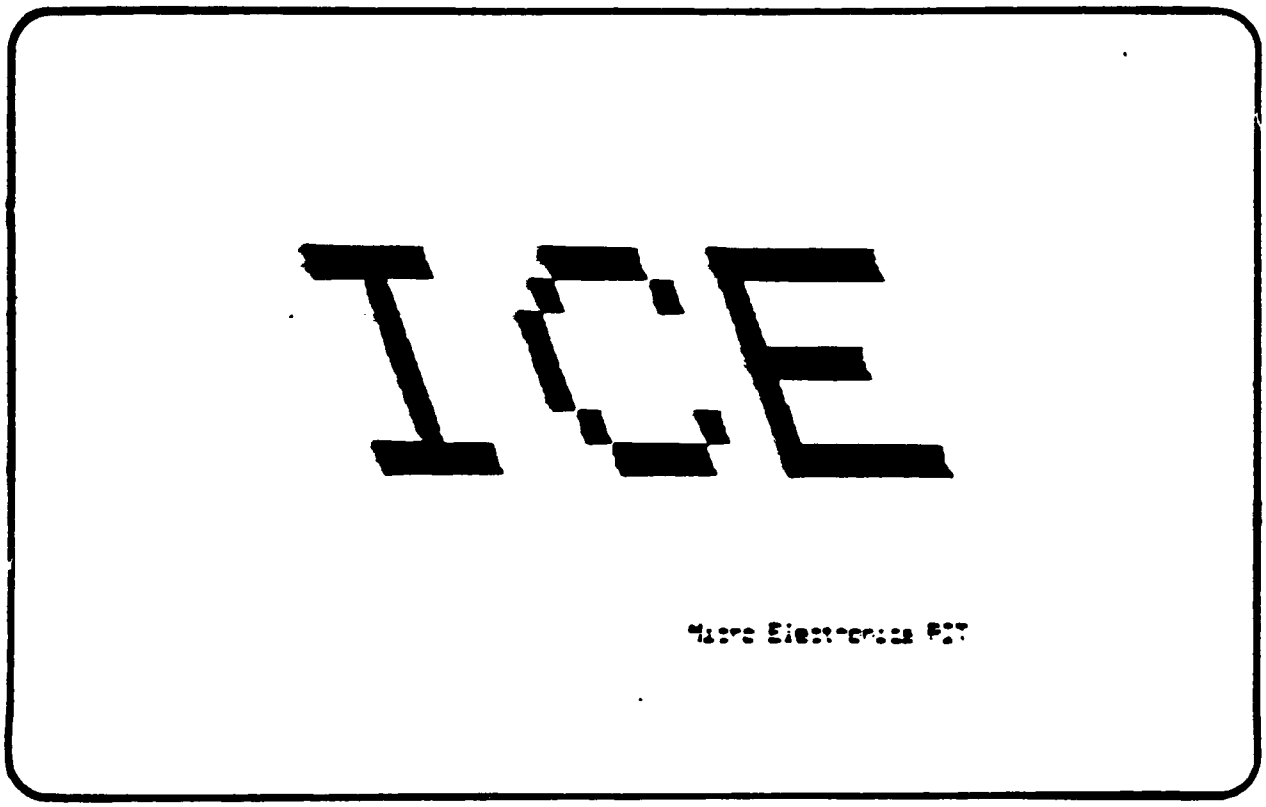
MANN [fn] [layer name] - Creates files used to make masks for fabrication. One file required for each level

CURSOR RESOLUTION

To change the movement step of the cursor hit 1-1um, 2-10um, 3-100um or 4-1000um steps whenever the cursor appears on the screen. When ICE is first started it will come up in 50um steps.

HINTS:

- Do not use the arrow keys to repeat commands.
- Make sure the design is selected before it it saved.
- Instead of using PROJOUT place a 1um by 1um box, on any layer, on the lower left corner of the design space.
- Make sure to burst an old design when bringing it into a design space. If this is not done, revisions cannot be make on previous work.
- For very large designs show only one or two layers when resetting to move to a different section of the design. This saves redrawing time.
- Bring in extraneous sections such as resolution targets and alignment marks last. This will again save on redrawing time.
- The upper right blue box shows the area of the design space being used.


ICE

ICE is an acronym for Integrated Circuit Editor. The program was created by Taylor Hogan during the 1984-1985 academic year. Since then, Taylor has made many enhancements resulting in the current version of ICE.

This manual was written by Tom Nutting as part of his M.S. Degree requirements.

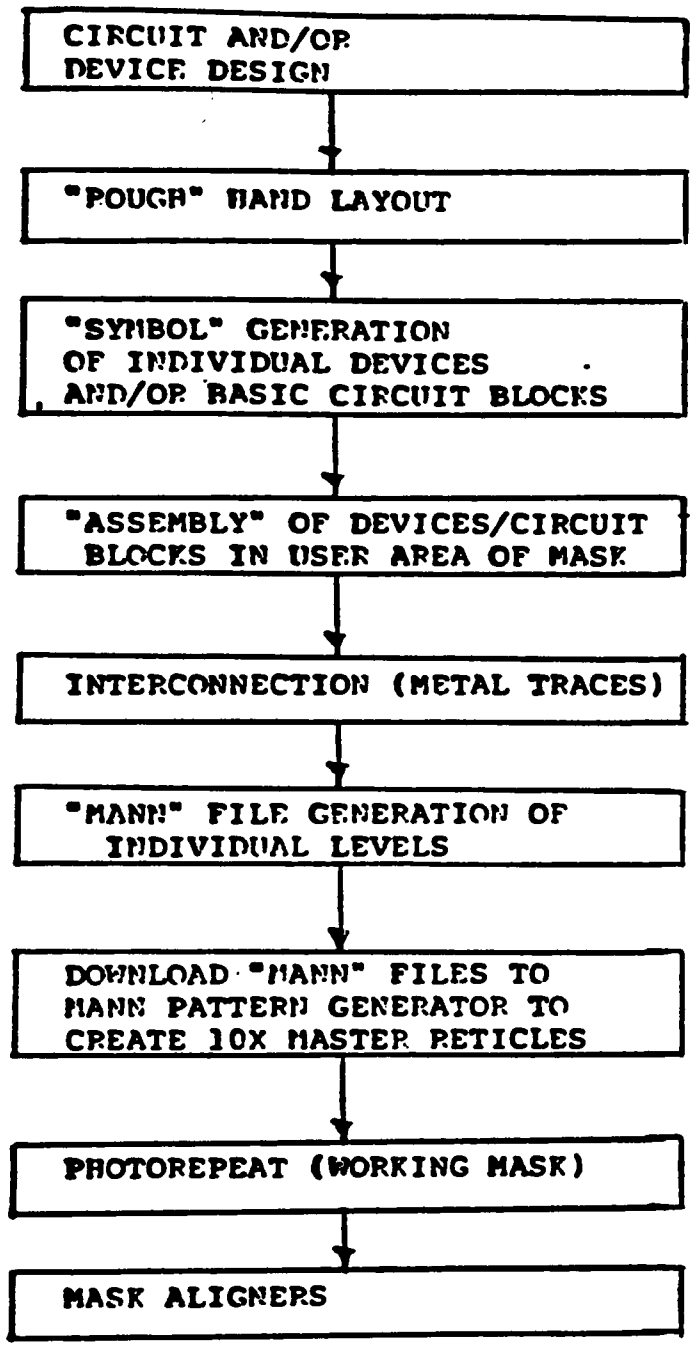
INTRODUCTION

The Integrated Circuit Editor (ICE) program provides the means for a user to create "artwork" necessary for integrated circuit layouts.The program resides on a mainframe computer and is accessed through graphics terminals on a time sharing basis, allowing simultaneous access by several users.

ICE uses Caltech Intermediate Format (CIF) to store data, this allows for an interface capability to any pre or post processors which utilize CIF format. A post processor which has been designed to interface with ICE is the MANN generator. This program transforms the CIF file into a MANN format file which subsequently controls a MANN mask generator.

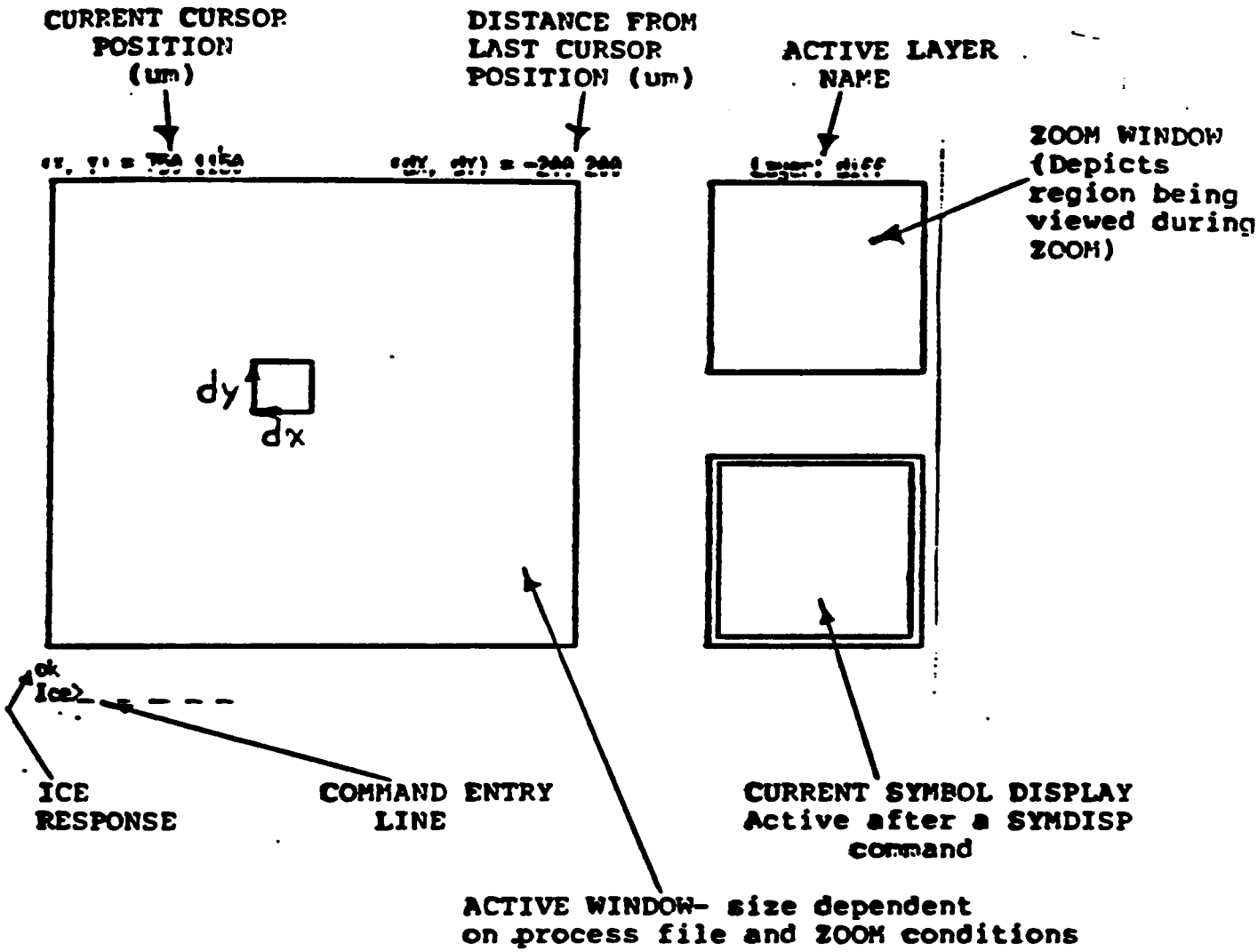
Designing IC masks via ICE is based on a heirarchal philosophy, primitive symbols (rectangles) are grouped to form more complex structures. These structures can then be saved in and recalled from the users disk storage area. There are several commands available to the user which allow a variety of linear transformations (move,clone,mirror,rotate,etc.) to be performed on these "symbols".

ICE Syster Flow Chart



ICE SCREEN DESCRIPTION

This is the CRT screen as viewed on a graphics terminal.



FILES UTILIZED BY ICE

There are three basic file types the user has interaction with when using ICE; Process files, CIF files and MANN files. Appendix A,B,and C contain full descriptions and examples of these files, the following is a summary of each file type.

PROCESS FILES:

A process file is a user selected/created text file which defines a number of parameters required by ICE. These are chip width and height,layer names and antiregions,and the name(s) of any MANN file(s) which are to be included when generating "artwork" MANN files. The user is prompted to identify the process file to be used at the beginning of each ICE session.

CIF FILES:

There are two types of CIF files, symbol and project. A symbol file contains the information required by ICE to construct a single symbol, such as a transistor. This single symbol may be a grouping of many graphical primitives (rectangles) which reside on more than one layer.

A project file contains all of the information pertaining to a particular project,such as a fully integrated opamp.The project file usually contains many different symbols - transistors,metal traces,registration marks,graphics,etc.

CIF files are readable, they may also be editted so that a scaling of geometries takes place.

MANN FILES:

A MANN file contains the information required by a MANN pattern generator to properly expose a reticle to be used in IC mask fabrication. The MANN file is generated from a CIF file and pertains to only one layer of a project. The MANN file is readable,containing a series of "flash" instructions which control the (x,y) location,the width and height,and the angle of each exposure.

COMMANDS

here are six basic command types in ICE, they are categorized as follows:

Graphical Primitives- commands which create the most basic types of cells.

Symbol Editing- commands which allow the user to perform a number of different linear transformations on symbols such as moving, copying and rotating so that higher level symbols can be created.

Screen Commands- control the scale and content of the information being displayed.

Cursor Resolution- control the resolution of the cursor step when using the arrow keys.

File Management- provide for the reading and writing of CIF files from/to memory.

Post Processors- provide for additional processing of CIF files such as MANN file generation and PLOT file generation.

The following pages describe the currently available commands in each of these categories.

The command syntax is as follows:

UPPER_CASE = command
lower_case = required arguement
[x,y,z] = one of x,y or z required
< > = optional arguement

BOX <layer_name>

The BOX command allows the user to create a rectangle of specific height, width and location on the currently defined layer. If the optional layer_name is specified, the layer will be changed to that specified, and the rectangle will be drawn on this new layer.

The BOX command prompts the user for:
1] The first corner of the rectangle,
2] The diagonal corner of the rectangle.

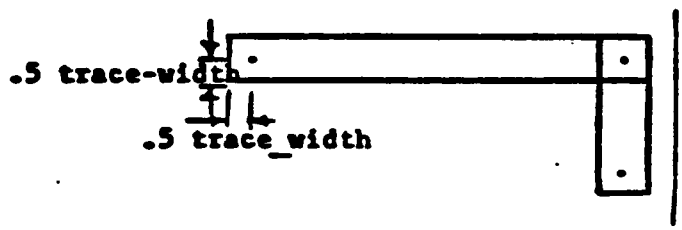
The (X,Y) position readouts become active upon the initiation of the BOX command, aiding the user in positioning the first corner of the rectangle. The return key then locks in this first corner position, and the (dx,dy) display is reset to 0,0. The arrow keys and optional cursor resolution keys are then used to obtain the desired width and height of the box. The (dx,dy) display shows the distance the cursor is from the first corner location. The return key is used to lock in the second (diagonal) corner of the box, terminating the BOX command.

TRACE trace_width <layer_name>

The TRACE command is used to draw paths of rectangles, the width of the trace being the required arguement trace_width, which is in um. This command is very useful for interconnecting various devices on a circuit.

The TRACE command prompts the user for:
1] The beginning of the trace,
2] The end of the trace.

The (X,Y) and (dx,dy) displays are active during a trace command, aiding the user in determining trace length and position. The trace will be located with respect to its' beginning and ending points as shown below.



The TRACE command is limited to drawing stricly horizontal and vertical rectangles.

The system will continue to prompt for beginning and ending points until the user specifies identical beginning and ending points. If continuous traces are desired, then the beginning point of the continuation should be specified to be the end point of the previous trace.

The width of the trace can only be modified by entering a new trace command with another width specification.

SELECT <layer_name> <layer_name> <layer_name> ...

The select command allows the user to specify the current set of selected symbol(s), the optional layer name arguement(s) provides for the capability of selecting only those symbol(s) resident in the specified layer(s).

The SELECT command prompts the user for:

1] The first corner of the select area,
2] The second (diagonal) corner of the select area.

The symbols that lie totally within the specified rectangular "bounding box" become the current set of selected symbols.The SELECT command selects symbols from all layers contained within the box if no layer_name(s) is(are) specified The system will report the number of symbols that it finds to be within the described rectangle.

The select command is often used before other symbol edit commands in order to specify which symbol (or symbols) is (are) to be editted. If more than one symbol is to be further editted, these must be GROUPed first.

GROUP

The GROUP command will always immediately follow a SELECT command, its' function is to integrate all of the selected symbols into one new symbol.This is used when multiple symbols form the basis of a new symbol. The GROUPed symbol becomes the current selected symbol.

BURST

The BURST command is used to logically break the currently selected symbol down one level of GROUPing. Multiple BURST commands may be required to break a symbol down to its' most prinitive forms, depending upon how the symbol was created. Only one symbol may be selected to be burst at a time, only complex (ie. previously grouped) symbols may be BURSTed.

MOVE

The MOVE command changes the location of the currently selected symbol.

The MOVE command prompts the user for:

1] The new lower left corner of the symbol.

The new position for the symbol may be specified prior to executing the MOVE command by using the POSITION command, or after prompting by using the arrow and cursor resolution keys. The symbol is moved after keying in a RET.

DELETE

The DELETE command removes the currently selected symbol from the design. Only one symbol may be deleted at a time, the currently selected symbol is undefined after the DELETE command executed.

CLONE

The CLONE command is used to copy the currently selected symbol into other regions of the design.

The CLONE command prompts the user for:

1) The new lower left corner of the clone item.

The new position for the clone item may be specified prior to executing the command by using the POSITION command, or after prompting by using the arrow and cursor resolution keys. A RET places the cloned item at the new location, and the system prompts for a new lower left corner position. This allows for multiple cloning of the same symbol in many locations. The CLONE command is terminated by CLONEing a symbol in the same location twice.

POSITION x y

The POSITION command allows the user to specify the current location of the cursor. The required arguements x y are the Cartesion coordinates of the desired cursor location in um. This command is useful for determining the exact starting location for the BOX and TRACE commands, and the exact desired location for MOVEing or CLONEing a symbol to.

ORIENT [1,2,3]

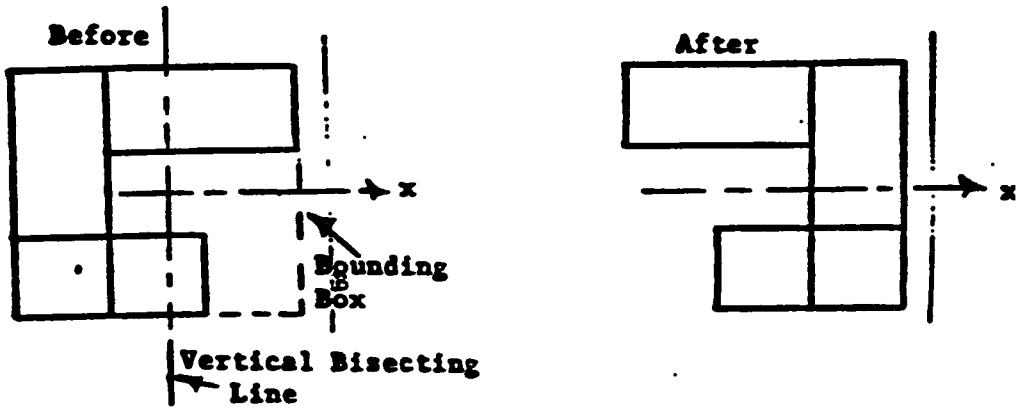
The ORIENT command will rotate the currently selected symbol about the center of its' "bounding box" through one of three possible angles. These angles are:

1: 90 degrees ccw
2: 180 degrees ccw
3: 270 degrees ccw

The currently selected symbol becomes the reORIENTed symbol after execution of this command.

MX

The MX command "mirrors" the currently selected symbol along the X axis (or about the Y axis). The symbol is mirrored about a vertical line bisecting the "bounding box" of the symbol. The figure below depicts the operation of this command.



The currently selected symbol becomes the "mirrored" symbol after execution of this command.

MY

The MY command is the same as the MX command except that the symbol is mirrored about a horizontal line bisecting the "bounding box" of the symbol.

LAYER layer_name

The LAYER command defines the current layer , all subsequent graphical primitives will be drawn on this layer. The current layer name is shown in the upper right hand corner of the screen. The current layer can be changed by either issuing a new LAYER command or by specifying the optional layer_name when using the BOX or TRACE commands.

SCREEN COMMANDS

ZOOM <scale_factor>

The ZOOM command allows the user to zoom in or out on a particular region of the design so that a more detailed view can be obtained. The optional scale factor lets the user specify the amount of magnification to be used. The scale_factor must be an integer, either positive or negative. Positive scale_factors magnify, negative scale_factors de-magnify. The default value for scale_factor is +2.

The ZOOM command prompts the user for:

1] The center of the desired window.

The center of the desired window is transformed into the center of the magnified or de-magnified window, the window is a square box.

RESET

The RESET command redraws the design at zoom factor 1, ie., the original scale_factor.

REDRAW

The REDRAW command redraws the design at the current scale_factor.

SHOW <layer_name> <layer_name> <layer_name> ...

The SHOW command redraws the design at the current scale_factor, but only those layers specified will be shown. This is very useful in reducing the clutter on the screen when working on only one or two layers of interest. Any number of layers may be selected,when no layer_name(s) is (are) specified all layers are shown.

If a primitive command is executed on a layer not specified by the latest SHOW command, the new symbol will not be visible.

SYMDISP

The SYMDISP command allows the user to see the currently selected symbol in the lower right display window of the screen. The symbol is displayed such that its' "bounding box" just fits inside of the display window, therefore it is not at the same scale_factor as the rest of the design. Any subsequent commands disable the SYMDISP function.

,2,3,4]

The cursor resolution commands set the current dimension the cursor will move when an arrow key is pressed. The values' associated with each of the arguements are:

1: 1 micron
2: 10 microns
3: 100 microns
4: 1000 microns

The resolution can be changed in any sequence desired, these commands are only used in conjunction with the arrow keys. The last resolution selected remains in effect until a new value is selected.

Example:

To move the cursor to the right by 436 microns, key in the following sequence-

3→→→→ 2→→→ 1→→→→→→
100um*4 10um*3 1um*6

FILE MANAGEMENT

PROJIN file_name

The PROJIN command will retreive the CIF project file specified by file_name, and place it into the ICE workspace. Anything currently existing in the ICE workspace will be deleted. A project file may consist of several symbols, and is usually an entire design.

PROJOUT file_name

The PROJOUT command will save the current design residing in the ICE workspace in the CIF project file specified by file_name.CIF. The ICE workspace will remain unaffected.

SYMIN file_name

The SYMIN command will retreive the CIF symbol file specified by file_name, and place it into the ICE workspace.

The SYMIN command will prompt the user for:

1] The lower left corner of the new symbol.

The lower left corner of the symbol may be specified prior to execution of the SYMIN command by using the POSITION command, or after execution by using the arrow keys and optional cursor resolution keys. The RET key terminates the SYMIN command, and places the symbol at the desired location.

SYMOUT file_name

The SYMOUT command stores the currently selected symbol into a CIF symbol file specified by file_name.CIF. Only one symbol may be saved with a SYMOUT command. This command is used when building a library of symbols that will be used repetetively.

) file_name layer_name

The MANN command will generate a MANN format file of the layer in the current design specified by layer_name.This will be stored in the file specified by file_name,the name of the stored file will be file_name.MAN. The MANN format file will provide the means for communicating the information required by the MANN PATTERN GENERATOR to expose 10X master reticles.

(Also see APPENDIX C)

PLOT file_name <layer_name> <layer_name> ...

The PLOT command will generate a PLOT format file of the layer in the current design specified by layer_name. This will be stored in the file specified by file_name, the name of the stored file will be file_name.PLT.

CURRENTLY UNAVAILABLE

CELL LIBRARY

The cell library is a collection of device designes that have been used in the past and have been characterized. These devices can range from individual transistors or resistors to operational amplifies or differential amplifiers. These cells can be used as building blocks (macrocells) in other circuits. When in ICE use the command "SYMIN filename" without quotes. The cell file must be in your account. Current cells are located in the department computer account MICROLIB. To copy these files to your account type

COPY USER7:MICROLIB.ICE.BIPOLARfilemane.extension *.*;*

The filenames should all begin with NWELL. For example:

NWELL_SMALLNPN.CIF
NWELL_SMALLPNP.CIF
NWELL_TESTDEVICES.CIF
NWELL_PADS.CIF
NWELL_30000HM.CIF

Using the NWELL*.CIF for filename.extension will result in a copy of all files. The extension CIF stands for Cal Tech Intermediate Form which is a standard format for storing layout data. When using the SYMIN command in the ICE editor the extension .CIF is not used.

There are 36 CIF files that can be used to create letters and numbers for labeling your layout. These are called Z#.CIF where # is the number 0 to 9 or letter A to Z. These may also be copied to your account for your use.

ROCHESTER INSTITUTE OF TECHNOLOGY - MICROELECTRONIC ENGINEERING
N-WELL BIPOLAR INTEGRATED CIRCUIT DESIGN MANUAL

SPICE PARAMETERS: NPN BIPOLAR TRANSISTOR

	PARAMETER		NPN SMALL	
1	IS	TRANSPORT SATURATION CURRENT	5.86E-15	A
2	BF	IDEAL MAXIMUM FORWARD BETA	120	-
3	NF	FORWARD CURRENT EMISSION COEFFICIENT	1.069	-
4	VAF	FORWARD EARLY VOLTAGE	-75.0	V
5	IKF	CORNER FOR FORWARD BETA HIGH CURRENT	800E-6	A
6	ISE	B-E LEAKAGE SATURATION CURRENT	3.00E-15	A
7	NE	B-E LEAKAGE EMISSION COEFFICIENT	1.591	-
8	BR	IDEAL MAXIMUM REVERSE BETA	0.959	-
9	NR	REVERSE CURRENT EMISSION COEFFICIENT	1	-
10	VAR	REVERSE EARLY VOLTAGE	6.14	V
11	IKR	CORNER FOR REVERSE BETA ROLL-OFF	2.69E-3	A
12	ISC	B-C LEAKAGE SATURATION CURRENT	2.09E-15	A
13	NC	B-C LEAKAGE EMISSION COEFFICIENT	1.04	-
14	RB	ZERO BIAS RESISTANCE	600	OHMS
15	IRB	CURRENT WHERE BASE RESISTANCE HALF	NA	A
16	RBM	MINIMUM BASE RESISTANCE AT HIGH I	NA	OHMS
17	RE	EMITTER RESISTANCE	8.18	OHMS
18	RC	COLLECTOR RESISTANCE	2 k	OHMS
19	CJE	B-E AERO BIAS DEPLETION CAPACITANCE	5.39E-13	F
20	VJE	B-E BUILT IN VOLTAGE	.987	V
21	MJE	B-E JUNCTION EXPONENTIAL FACTOR	0.362	-
22	TF	IDEAL FORWARD TRANSIT TIME	3.36E-10	SEC
23	XTF	COEFFICIENT FOR BIAS DEPENDENCE OF TF	NA	-
24	VTF	VOLTAGE DESCRIBING VBC DEPENDENCE TF	NA	V
25	ITF	HIGH CURRENT PARAMETER EFFECT ON TF	NA	A
26	PTF	EXCESS PHASE AT W=1/TF	NA	DEG
27	CJC	B-C ZERO BIAS DEPLETION CAPACIATANCE	1.14E-12	F
28	VJC	B-C BUILT-IN VOLTAGE	.753	V
29	MJC	B-C JUNCTION EXPONENTIAL FACTOR	0.177	-
30	XCJC	FRACTION OF B-C DEPLETION CAPACITANCE	1	-
31	TR	IDEAL REVERSE TRANSIT TIME	5.0E-9	SEC
32	CJS	ZERO BIAS C-SUB CAPACITANCE	1.8E-12	F
33	VJS	SUB JUNCTION BUILT IN VOLTAGE	.662	V
34	MJS	SUB JUNCTION EXPONENTIAL FACTOR	0.318	-
35	XTB	BETA TEMPERATURE EXPONENT (BF & BR)	0	-
36	EG	ENERGY GAP FOR TEMP EFFECT ON IS	1.1	EV
37	XTI	TEMP COEFFICIENT EFFECT ON IS	3	-
38	KF	FLICKER-NOISE COEFFICIENT	0	-
39	AF	FLICKER-NOISE EXPONENT	1	-
40	FC	COEFFICIENT FOR FORWARD DEP CAP	0.5	-

ROCHESTER INSTITUTE OF TECHNOLOGY - MICROELECTRONIC ENGINEERING
N-WELL BIPOLAR INTEGRATED CIRCUIT DESIGN MANUAL

SPICE PARAMETERS: PNP BIPOLAR TRANSISTOR

	PARAMETER		PNP SMALL	
1	IS	TRANSPORT SATURATION CURRENT	9E-15	A
2	BF	IDEAL MAXIMUM FORWARD BETA	40	-
3	NF	FORWARD CURRENT EMISSION COEFFICIENT	1.069	-
4	VAF	FORWARD EARLY VOLTAGE	120	V
5	IKF	CORNER FOR FORWARD BETA HIGH CURRENT	800E-6	A
6	ISE	B-E LEAKAGE SATURATION CURRENT	3.00E-15	A
7	NE	B-E LEAKAGE EMISSION COEFFICIENT	1.591	-
8	BR	IDEAL MAXIMUM REVERSE BETA	0.959	-
9	NR	REVERSE CURRENT EMISSION COEFFICIENT	1	-
10	VAR	REVERSE EARLY VOLTAGE	6.14	V
11	IKR	CORNER FOR REVERSE BETA ROLL-OFF	2.69E-3	A
12	ISC	B-C LEAKAGE SATURATION CURRENT	2.09E-15	A
13	NC	B-C LEAKAGE EMISSION COEFFICIENT	1.04	-
14	RB	ZERO BIAS RESISTANCE	2 k	OHMS
15	IRB	CURRENT WHERE BASE RESISTANCE HALF	NA	A
16	RBM	MINIMUM BASE RESISTANCE AT HIGH I	NA	OHMS
17	RE	EMITTER RESISTANCE	200	OHMS
18	RC	COLLECTOR RESISTANCE	2 k	OHMS
19	CJE	B-E AERO BIAS DEPLETION CAPACITANCE	5.39E-13	F
20	VJE	B-E BUILT IN VOLTAGE	.753	V
21	MJE	B-E JUNCTION EXPONENTIAL FACTOR	0.362	-
22	TF	IDEAL FORWARD TRANSIT TIME	2.0E-10	SEC
23	XTF	COEFFICIENT FOR BIAS DEPENDENCE OF TF	NA	-
24	VTF	VOLTAGE DESCRIBING VBC DEPENDENCE TF	NA	V
25	ITF	HIGH CURRENT PARAMETER EFFECT ON TF	NA	A
26	PTF	EXCESS PHASE AT W=1/TF	NA	DEG
27	CJC	B-C ZERO BIAS DEPLETION CAPACIATANCE	1.8E-12	F
28	VJC	B-C BUILT-IN VOLTAGE	.662	V
29	MJC	B-C JUNCTION EXPONENTIAL FACTOR	0.177	-
30	XCJC	FRACTION OF B-C DEPLETION CAPACITANCE	1	-
31	TR	IDEAL REVERSE TRANSIT TIME	5.0E-9	SEC
32	CJS	ZERO BIAS C-SUB CAPACITANCE	3.0E-12	F
33	VJS	SUB JUNCTION BUILT IN VOLTAGE	0.472	V
34	MJS	SUB JUNCTION EXPONENTIAL FACTOR	0.318	-
35	XTB	BETA TEMPERATURE EXPONENT (BF & BR)	0	-
36	EG	ENERGY GAP FOR TEMP EFFECT ON IS	1.1	EV
37	XTI	TEMP COEFFICIENT EFFECT ON IS	3	-
38	KF	FLICKER-NOISE COEFFICIENT	0	-
39	AF	FLICKER-NOISE EXPONENT	1	-
40	FC	COEFFICIENT FOR FORWARD DEP CAP	0.5	-

ROCHESTER INSTITUTE OF TECHNOLOGY - MICROELECTRONIC ENGINEERING
N-WELL BIPOLAR INTEGRATED CIRCUIT DESIGN MANUAL

SPICE PARAMETERS: JUNCTION FIELD EFFECT TRANSISTORS

	PARAMETER		P-CHANNEL JFET	UNITS
1	VTO	THRESHOLD VOLTAGE	2.0	V
2	BETA	TRANSCONDUCTANCE PARAMETER	1.25E-4	A/V**2
3	LAMBDA	CHANNEL LENGTH MODULATION	0.01	1/V
4	RD	DRAIN OHMIC RESISTANCE	100	OHM
5	RS	SOURCE OHMIC RESISTANCE	100	OHM
6	CGS	ZERO BIAS G-S JUNCTION CAP	2.0E-12	F
7	CGD	ZERO BIAS G-D JUNCTION CAP	0.5E-12	F
8	PB	GATE JUNCTION POTENTIAL	0.7	V
9	IS	GATE JUNCTION SATURATION CUR	1.0E-10	A
10	KF	FLICKER NOISE COEFFICIENT	-	-
11	AF	FLICKER NOISE EXPONENT	-	-
12	FC	COEFFICIENT FOR FORWARD-BIAS DEPLETION CAPACITANCE FORMULA	-	-

ROCHESTER INSTITUTE OF TECHNOLOGY - MICROELECTRONIC ENGINEERING
N-WELL BIPOLAR INTEGRATED CIRCUIT DESIGN MANUAL

SPICE PARAMETERS: METAL GATE PMOS FIELD EFFECT TRANSISTOR

	PARAMETER		P-MOSFET ENHANCEMENT	UNITS
1	LEVEL		1	-
2	VTO	ZERO-BIAS THRESHOLD VOLTAGE	-	V
3	KP	TRANSCONDUCTANCE PARAMETER	-	A/V**2
4	GAMMA	BULK THRESHOLD PARAMETER	-	V**0.5
5	PHI	SURFACE POTENTIAL	-	V
6	LAMBDA	CHANNEL-LENGHT MODULATION	3.05E-2	1/V
7	RD	DRAIN OHMIC RESISTANCE	-	OHM
8	RS	SOURCE OHMIC RESISTANCE	-	OHM
9	CBD	ZERO-BIASED B-D JUNCTION CAP	-	F
10	CBS	ZERO-BIASED B-S JUNCTION CAP	-	F
11	IS	BULK JUNCTION SATURATION CURRENT	-	A
12	PB	BULK JUNCTION POTENTIAL	-	V
13	CGSO	GATE SOURCE OVERLAP CAPACITANCE	1.6E-10	F/M
14	CGDO	GATE DRAIN OVERLAP CAPACITANCE	1.6E-10	F/M
15	CGBO	GATE BULK OVERLAP CAPACITANCE	1.7E-10	F/M
16	RSH	D&S DIFFUSION SHEET RESISTANCE	25.4	OHM/SQ
17	CJ	ZERO BIAS JUNCTION BOTTOM CAP/AREA	1.1E-4	F/M**2
18	MJ	BULK JUNCTION BOTTOM GRADING COEFF	0.5	-
19	CJSW	ZERO BIAS BULK JUNCTION SIDEWALL CAP	5.0E-10	F/M
20	MJSW	BULK JUNCTION SIDEWALL GRADING COEFF	0.33	-
21	JS	BULK JUNCTION SATURATION CURRENT/AREA	1E-12	A/M**2
22	TOX	OXIDE THICKNESS	635E-10	M
23	NSUB	SUBSTRATE DOPING	3.5E14	1/CM**3
24	NSS	SURFACE STATE DENSITY	0.5E11	1/CM**2
25	NFS	FAST SURFACE STATE DENSITY	6.03E11	1/CM**2
26	TPG	TYPE OF GATE	0	-
27	XJ	JUNCTION DEPTH	3.000U	M
28	LD	LATERAL DIFFUSION	3.000U	M
29	UO	SURFACE MOBILITY	241	CM**2/V
30	UCRIT	CRITICAL FIELD FOR MOBILITY	10000	V/CM
31	UEXP	CRITICAL FIELD EXPONENT FOR MOBILITY	7.46E-3	-
32	UTRA	TRANSVERSE FIELD COEFFICIENT	-	-
33	VMAX	MAXIMUM DRIFT VELOCITY	100000	M/S
34	NEFF	TOTAL CHANNEL CHARGE	1.00E-2	-
35	XQC	THIN OXIDE FLAG	-	-
36	KF	FLICKER NOISE	-	-
37	AF	FLICKER NOISE EXPONENT	-	-
38	FC	COEFF FORWARD BIAS DEPLETION CAP	-	-
39	DELTA	WIDTH EFFECT ON THRESHOLD VOLTAGE	1.037	-
40	THETA	MOBILITY MODULATION	-	1/V
41	STATIC	FEEDBACK	-	-
42	KAPPA	SATURATION FIELD FACTOR	-	-

STANDARD CELL LIBRARY LIST

_10PAD.CIF	Standard 10 pad layout
LL_PADS.CIF	40 pad layoout
LL_TESTDEVICES.CIF	Test devices surrounding chip layout
LL_SMALLPNP.CIF	Small geometry pnp vertical transistor
LL_NMOS.CIF	NMOS transistor, metal gate
LL_PMOS.CIF	PMOS transistor, metal gate
LL_IILNORAND.CIF	IIL nor/and gate
LL_SMALLNPN.CIF	Small geometry npn vertical transistor
LL_CURMIR.CIF	200 uA current mirror
LL_VERTPNP.CIF	Small substrate vertical pnp transistor
LL_DARLINGTON.CIF	An npn Darlington circuit
LL_DIFFAMP.CIF	A differential amplifier
LL_CNTRESX.CIF	Contact resistance structures
LL_RPLSXXX.CIF	Split cross structures
LL_XXXOHMB.CIF	Various base level resistors
LL_XXXOHME.CIF	Various emitter level resistors
LL_JFET.CIF	Junction field effect transistor
LL_OUTSTAGE.CIF	AB output stage
LL_PINCHX.CIF	Various pinch resistors
LL_OPAMP.CIF	Operational amplifier
LL_PNPLATX.CIF	Lateral PNP transistors
LL_ZX.CIF	Labelling letters a through z (replace X)
LL_Z1.CIF	Labelling numbers 1 through 0 (replace 1)
LL_120x210.CIF	Large npn transistor
LL_INVERT.CIF	Inverter circuit
_LVLSHFT.CIF	Levelshifter circuit
_RM.CIF	RIT symbol

ROCHESTER INSTITUTE OF TECHNOLOGY - MICROELECTRONIC ENGINEERING
N-WELL BIPOLAR INTEGRATED CIRCUIT DESIGN MANUAL

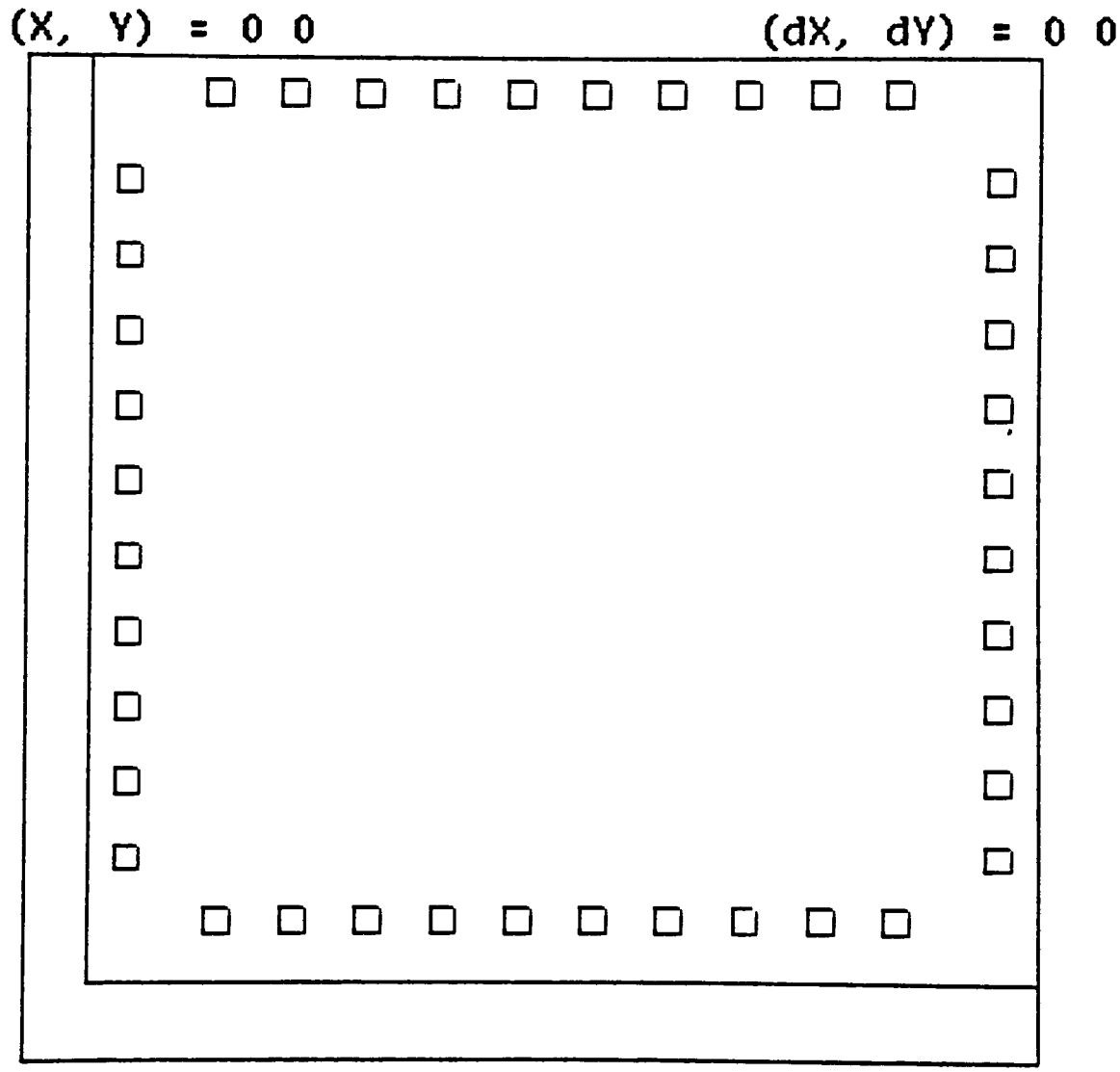
CELLNAME: NWELL_PADS.CIF

DESCRIPTION: These are the desired pad locations for automatic wafer testing.

CELL SIZE: 4000 by 4000 micrometer

CELL PLACEMENT: This cell must be placed at the origin x,y = (0,0)

LAYOUT:



ok
Ice> SYMOUT NWELL_PADS

ROCHESTER INSTITUTE OF TECHNOLOGY - MICROELECTRONIC ENGINEERING
N-WELL BIPOLAR INTEGRATED CIRCUIT DESIGN MANUAL

CELLNAME: NWELL_TESTDEVICES.CIF

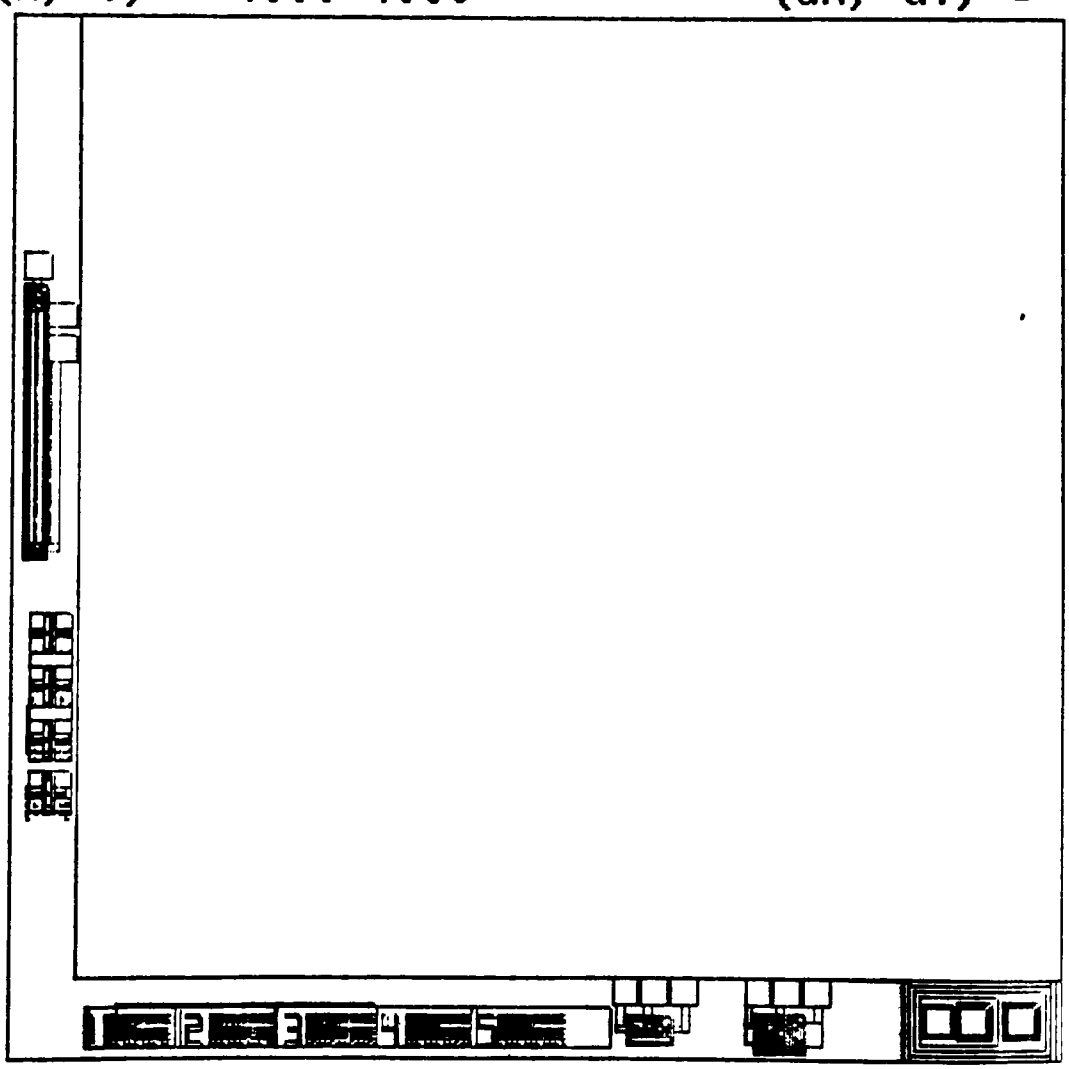
DESCRIPTION: This cell contains the alignment marks, resolution targets, and test devices for the nwell bipolar process. It is 250 micrometers wide along the left side and 300 micrometers high along the bottom. The cell contains alignment marks, small npn, small pnp, 3000ohm resistor, large npn transistor and resolution target.

CELL SIZE: 200 BY 4000 AND 300 BY 4000 micrometer

CELL PLACEMENT: This cell must be placed at the origin x,y = (0,0)

LAYOUT:

(X, Y) = 4000 4000 (dX, dY) =



ok
Ice> SYMOUT NWELL_TESTDEVICES

ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING DEPARTMENT

N-WELL BIPOLAR INTEGRATED CIRCUIT DESIGN MANUAL

CELL NAME: NWELL_10PAD.CIF

DESCRIPTION:

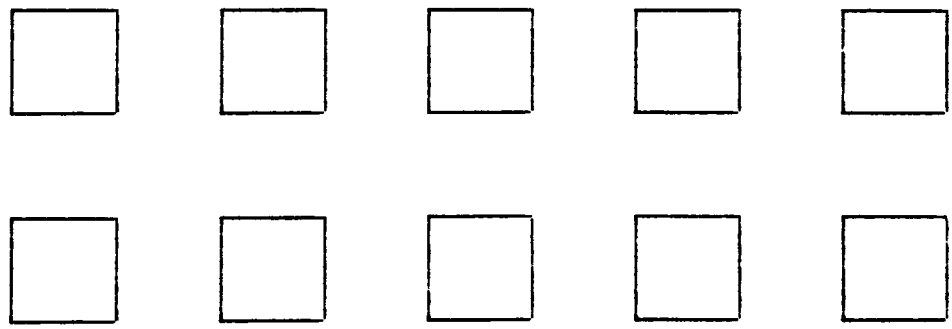
This is a standard 10 pad metal layout for use with a probe card.

CELL SIZE: 900 x 300 microns

CELL PLACEMENT:

OTHER INFORMATION:

LAYOUT:



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MICROELECTRONIC ENGINEERING DEPARTMENT

N-WELL BIPOLAR INTEGRATED CIRCUIT DESIGN MANUAL

CELL NAME: NWELL_CNTRESX.CIF and NWELL_RPLSXXX.CIF

DESCRIPTION:

These are contact resistance and Split-cross structure for the base or emitter levels.

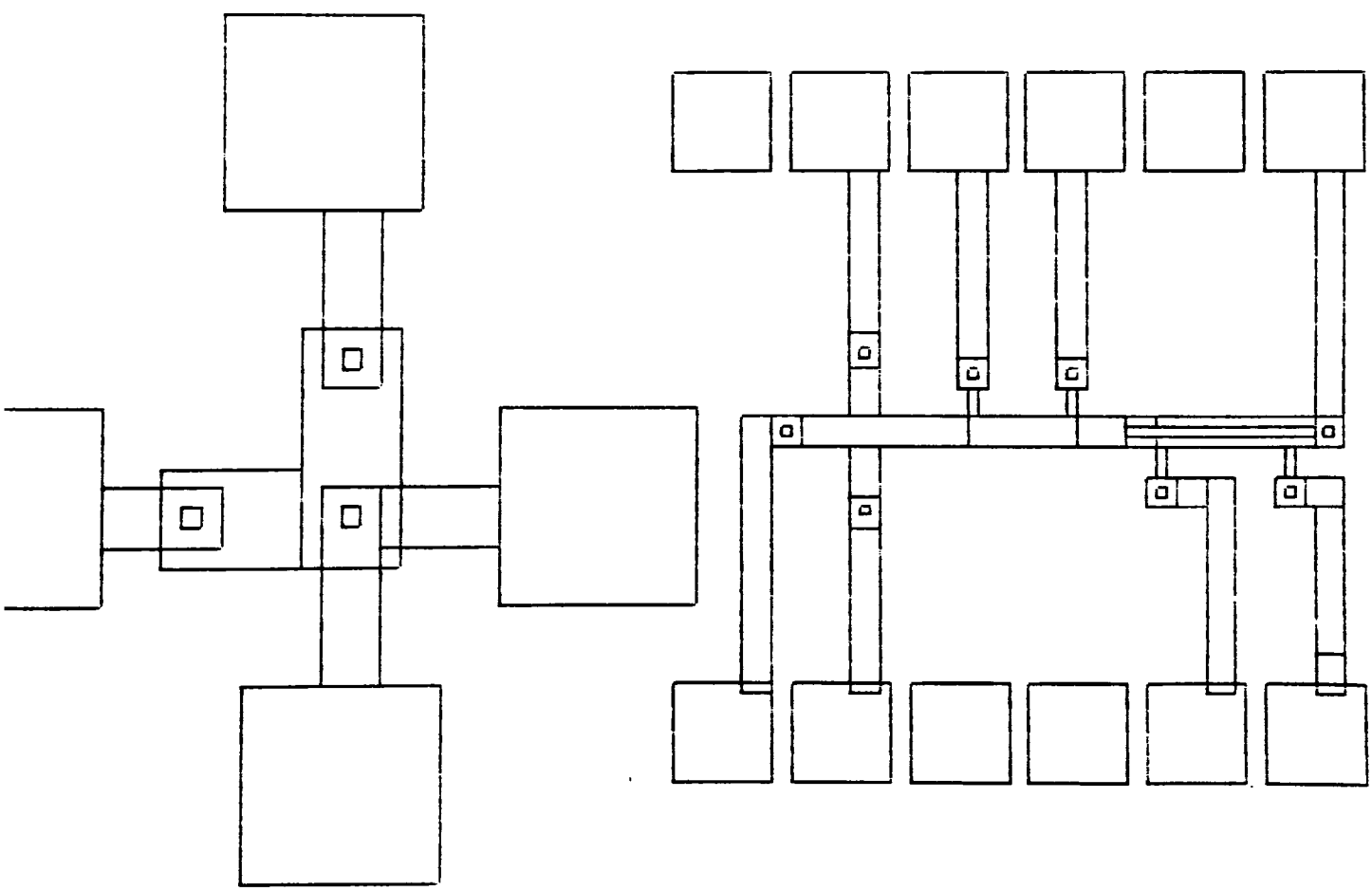
CELL SIZE: 350 x 350 microns contact, 750 x750 Splitcross

CELL PLACEMENT:

OTHER INFORMATION:

The emitter contact structure is NWELL_CNTRESE.CIF
The base contact structure is NWELL_CNTRESB.CIF
The emitter Splitcross is NWELL_RPLSEMITTER.CIF
The base Splitcross is NWELL_RPLSBASE.CIF

LAYOUT:



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N-WELL BIPOLAR INTEGRATED CIRCUIT DESIGN MANUAL

CELL NAME: NWELL_CURMIR.CIF

DESCRIPTION:

Attach Vcc to top left contact cut. Attach Vee to guardring. Mirror current lead runs through middle of resistor.

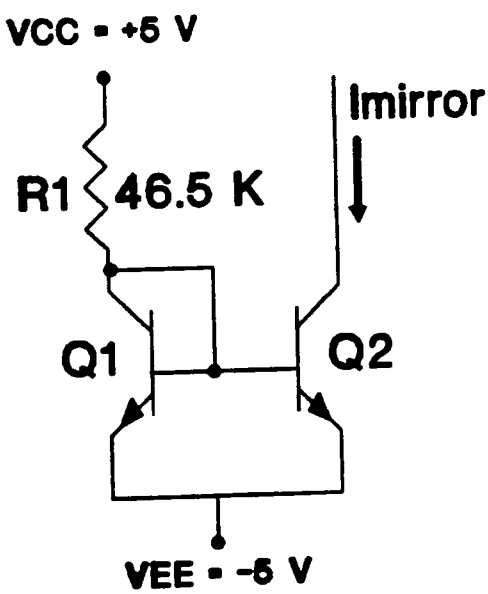
CELL SIZE: 380 x 510 microns

CELL PLACEMENT:

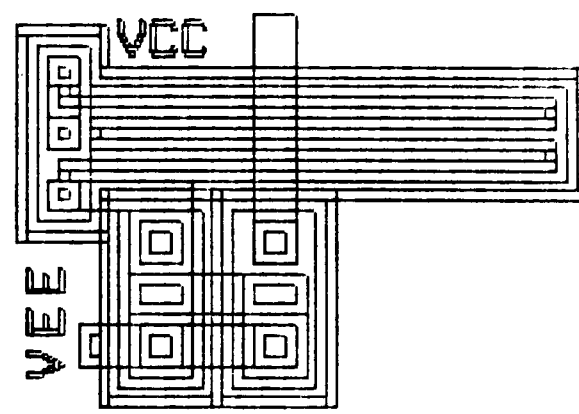
OTHER INFORMATION:

This is a current mirror designed as 200 microamp current source

SCHEMATIC



LAYOUT



ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING DEPARTMENT

N-WELL BIPOLAR INTEGRATED CIRCUIT DESIGN MANUAL

CELL NAME: NWELL_DARLINGTON.CIF

DESCRIPTION:

This is an NPN Darlington circuit and is used for high gain applications.

CELL SIZE: 180 x 210 microns

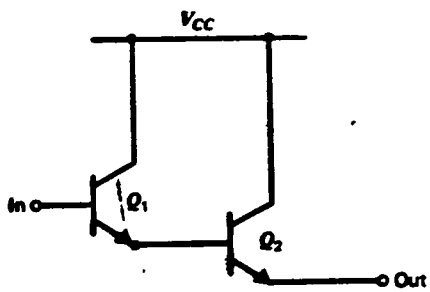
CELL PLACEMENT:

Guardrings can overlap other guardrings

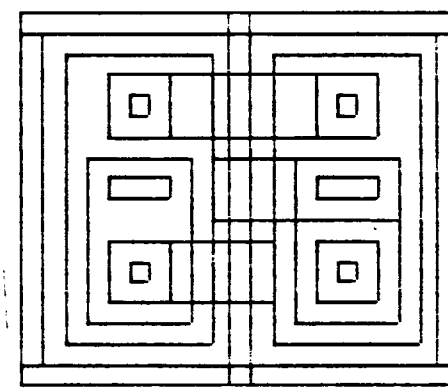
OTHER INFORMATION:

It is formed from two cascaded NPN transistors

SCHEMATIC



LAYOUT



ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING DEPARTMENT

N-WELL BIPOLAR INTEGRATED CIRCUIT DESIGN MANUAL

CELL NAME: NWELL_DIFFAMP.CIF

DESCRIPTION:

This circuit is a differential amplifier with pull-up resistors.

CELL SIZE: 470 x 470 microns

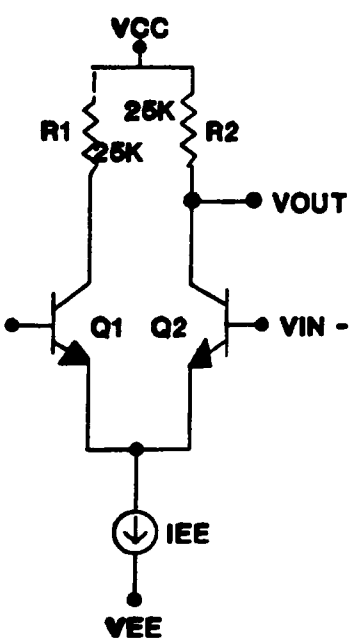
CELL PLACEMENT:

The positive supply voltage is on far right side of cell

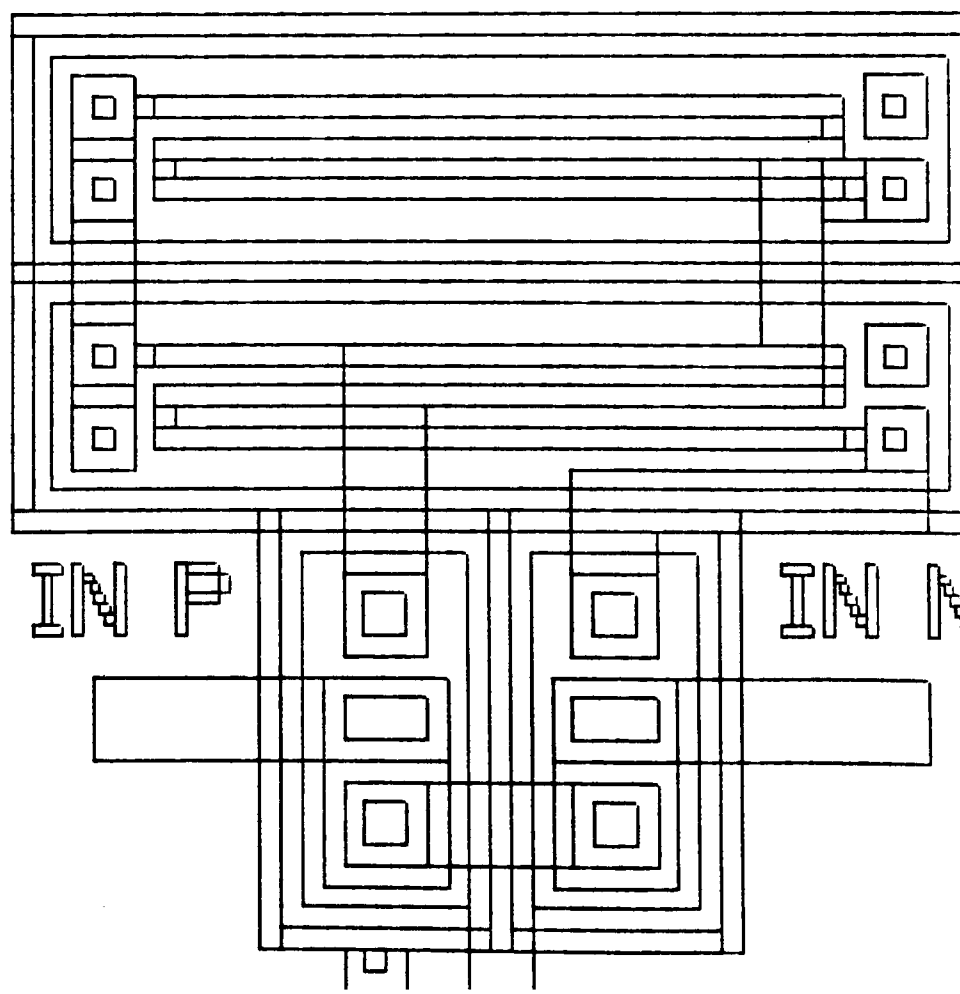
OTHER INFORMATION:

The pull-up resistors are 25kohm base and the transistors are NPN

SCHEMATIC



LAYOUT



ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING DEPARTMENT

N-WELL BIPOLAR INTEGRATED CIRCUIT DESIGN MANUAL

CELL NAME: NWELL_IILNORAND.CIF

DESCRIPTION:

This is a two input dual function nor/and gate.

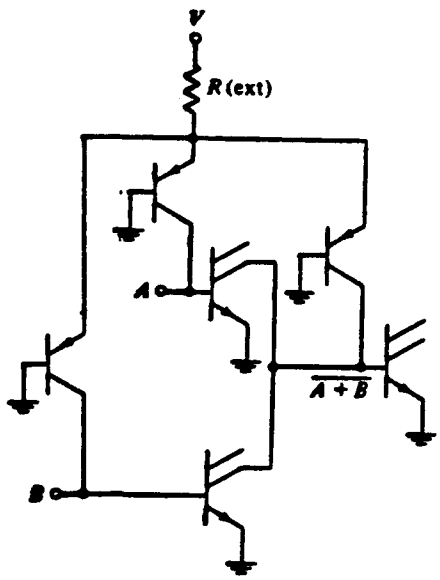
CELL SIZE: 350 x 400 microns

CELL PLACEMENT:

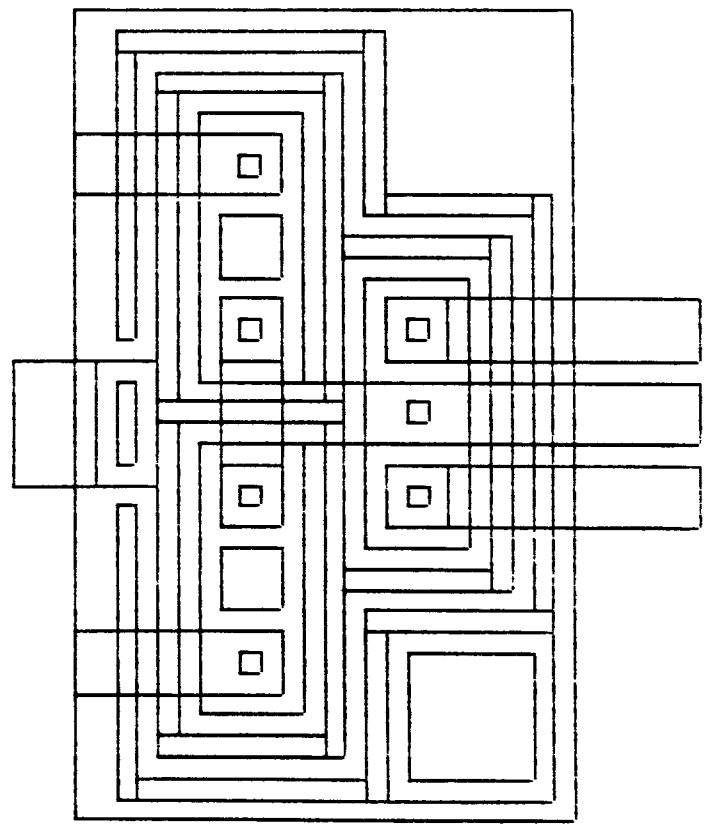
OTHER INFORMATION:

The middle output is the NOR function
The two other outputs are both the AND function

SCHEMATIC



LAYOUT



ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING DEPARTMENT

N-WELL BIPOLAR INTEGRATED CIRCUIT DESIGN MANUAL

CELL NAME: NWELL_JFET.CIF

DESCRIPTION:

This is a Junction Field Effect Transistor

CELL SIZE: 130 x 160 microns

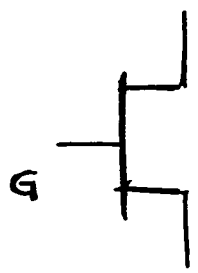
CELL PLACEMENT:

Guardring can overlap othe guardings

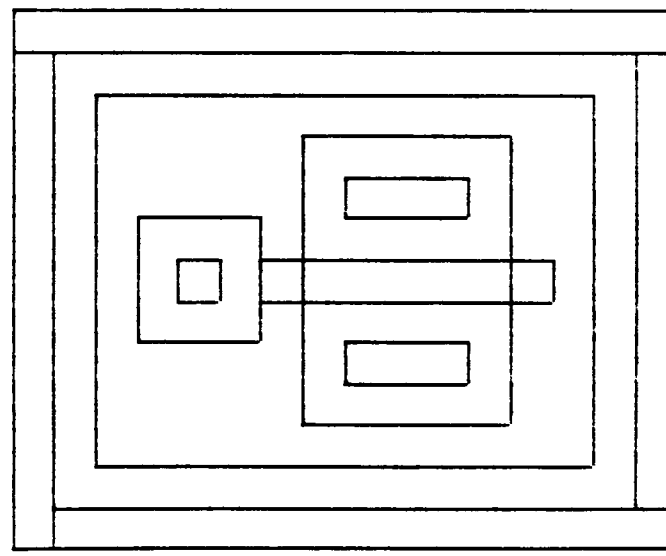
OTHER INFORMATION:

Gate is long diffusion in center of cell

SCHEMATIC



LAYOUT



ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING DEPARTMENT

N-WELL BIPOLAR INTEGRATED CIRCUIT DESIGN MANUAL

CELL NAME: NWELL_NMOS.CIF

DESCRIPTION:

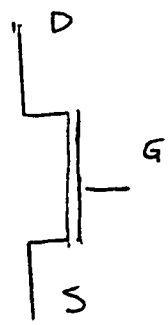
This is an NMOS transistor circuit located inside and N-well.

CELL SIZE: 90 X 150 microns

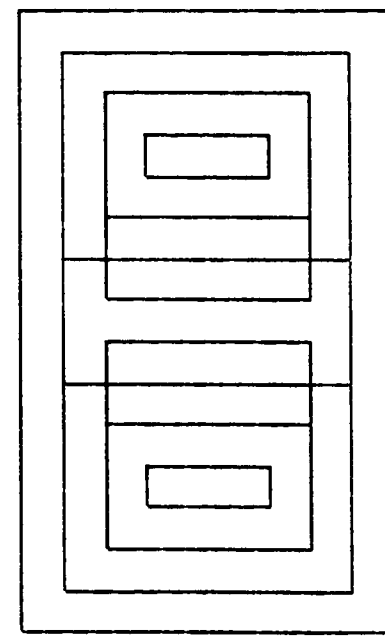
CELL PLACEMENT: The metal overlaps both sides of the gate region for either side access

OTHER INFORMATION:

SCHEMATIC



LAYOUT



ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING DEPARTMENT

N-WELL BIPOLAR INTEGRATED CIRCUIT DESIGN MANUAL

CELL NAME: NWELL_OPAMP.CIF

DESCRIPTION:

Operational amplifier using two cascaded differential amplifiers and pull-up resistors

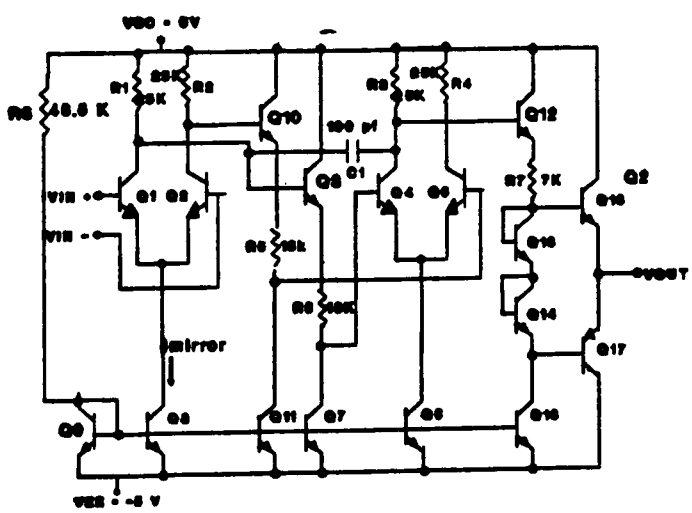
CELL SIZE: 2000 um by 1200 um

CELL PLACEMENT:

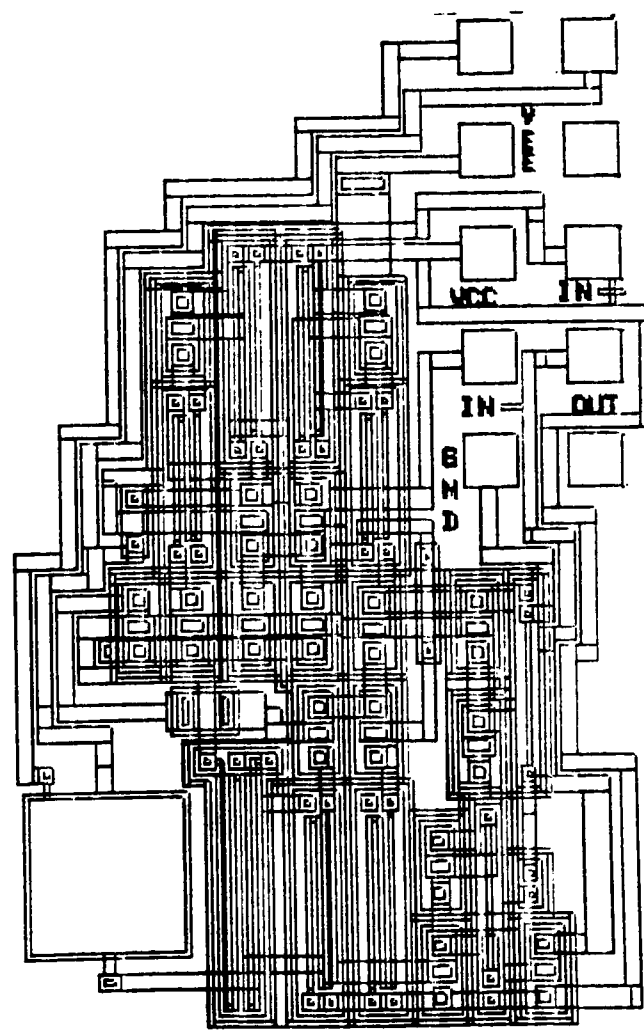
OTHER INFORMATION:

Gain is designed for 3600 in full differential mode

SCHEMATIC



LAYOUT



ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING DEPARTMENT

N-WELL BIPOLAR INTEGRATED CIRCUIT DESIGN MANUAL

CELL NAME: NWELL_OUTSTAGE.CIF

DESCRIPTION:

This is an AB output stage

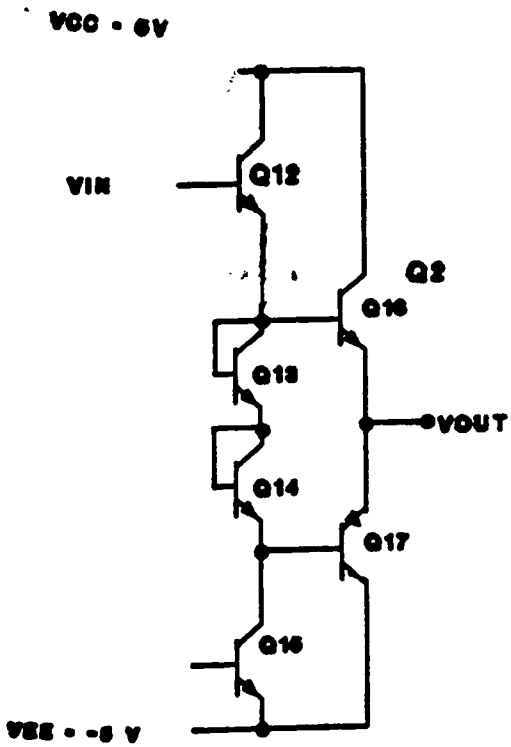
CELL SIZE: 400 x 500 microns

CELL PLACEMENT:

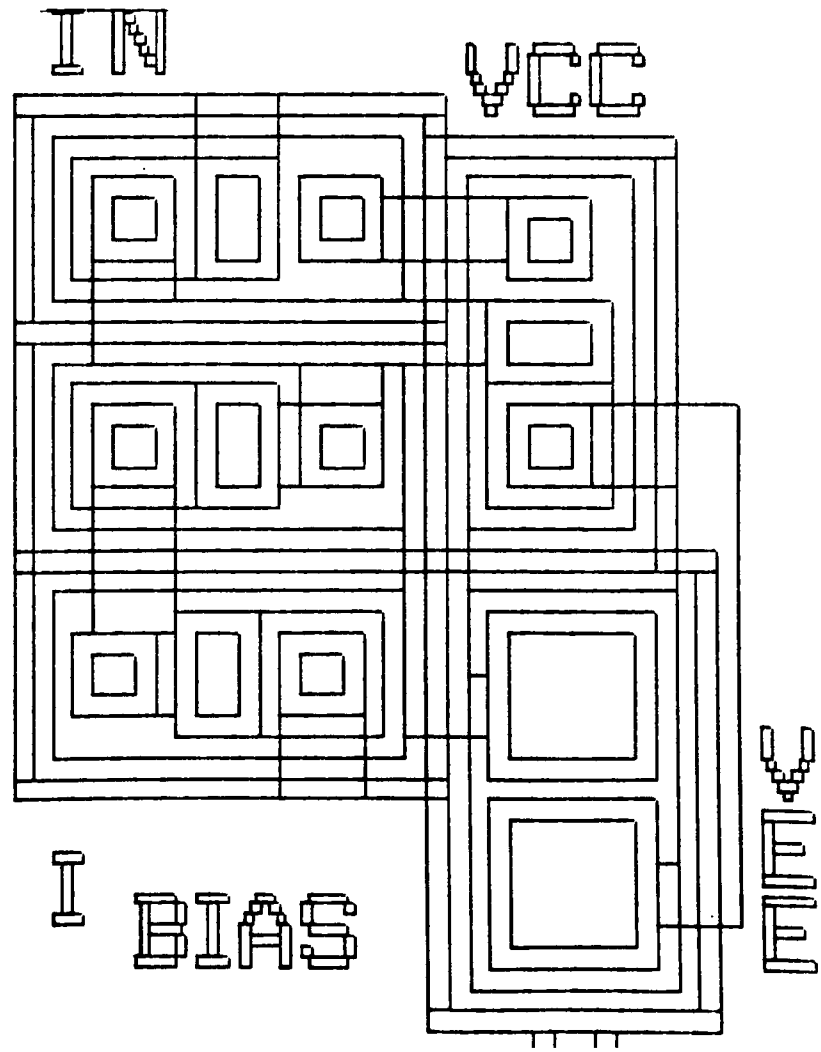
OTHER INFORMATION:

Attach positive supply to collector below Vcc symbol and Vee to guard ring. Ibias and input leads overlap guardring near lettering. Output is far right metal trace.

SCHEMATIC



LAYOUT



ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING DEPARTMENT

N-WELL BIPOLAR INTEGRATED CIRCUIT DESIGN MANUAL

CELL NAME: NWELL_PINCHXXX.CIF

DESCRIPTION:

Various pinch resistors, for high resistance uses

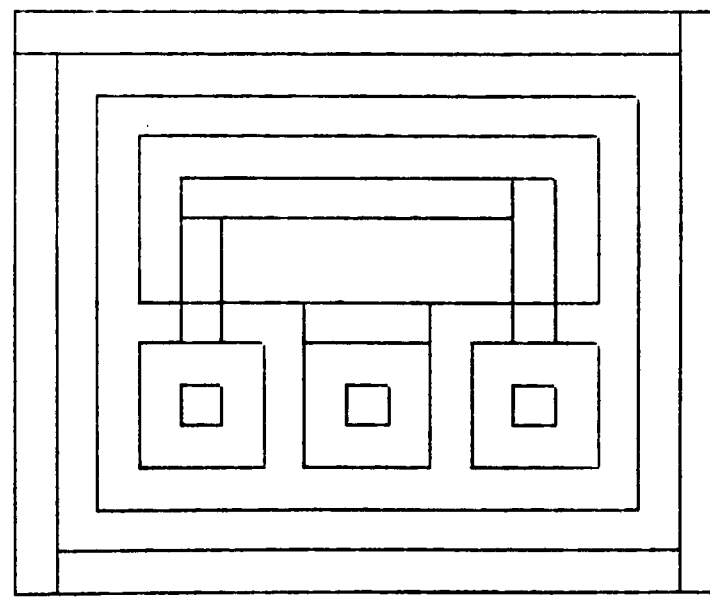
CELL SIZE:

CELL PLACEMENT:

OTHER INFORMATION:

SCHEMATIC

LAYOUT



ROCHESTER INSTITUTE OF TECHNOLOGY
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N-WELL BIPOLAR INTEGRATED CIRCUIT DESIGN MANUAL

CELL NAME: NWELL_PNPLATX.CIF

DESCRIPTION:

Lateral pnp transistors

CELL SIZE: 200 um by 130 um

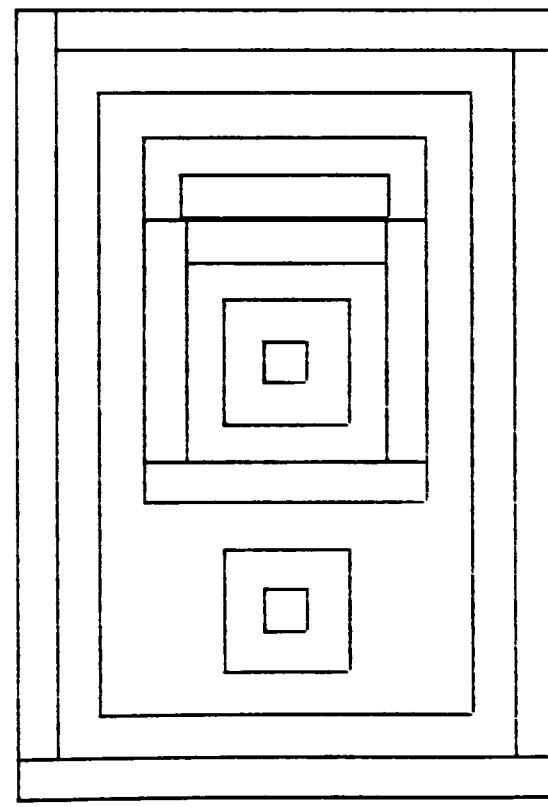
CELL PLACEMENT:

OTHER INFORMATION:

X defines the lithographic basewidth (6,7,8,9,10 um)

SCHEMATIC

LAYOUT



ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING DEPARTMENT

N-WELL BIPOLAR INTEGRATED CIRCUIT DESIGN MANUAL

CELL NAME: NWELL_SMALLNPN.CIF

DESCRIPTION:

This is a minimum geometry NPN vertical transistor with N-well isolation and p-type guard ring.

CELL SIZE: 180 x 110 microns

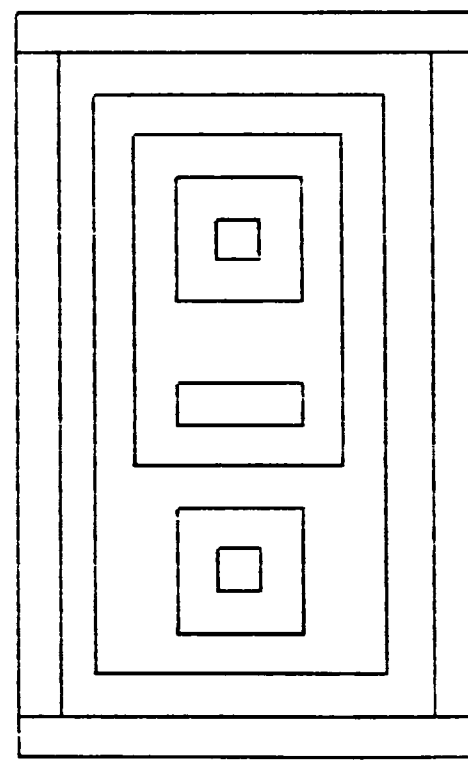
CELL PLACEMENT:

OTHER INFORMATION:

Beta = 100, BVceo=15 volts, Va=-90 volts, High level injection current limit is approximately 1 milliamp

SCHEMATIC

LAYOUT



ROCHESTER INSTITUTE OF TECHNOLOGY - MICROELECTRONIC ENGINEERING
N-WELL BIPOLAR INTEGRATED CIRCUIT DESIGN MANUAL

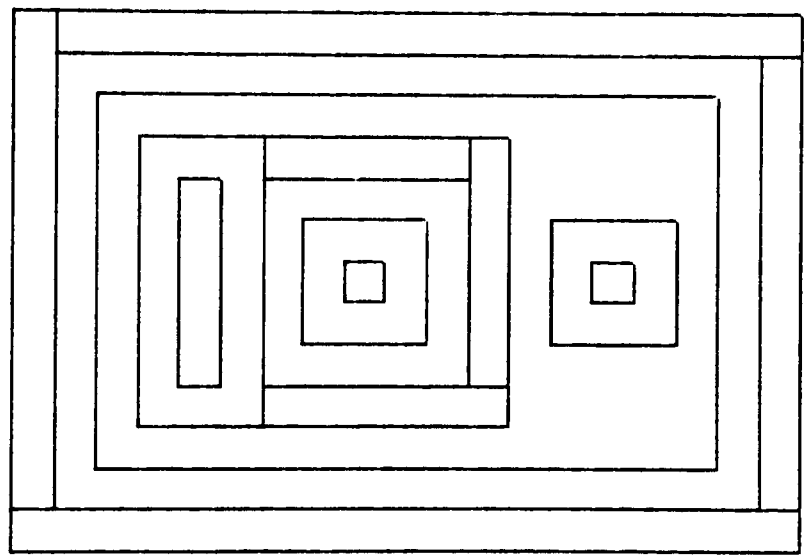
CELLNAME: NWELL_SMALLPNP.CIF

DESCRIPTION: This is a minimum area PNP lateral transistor with n-well and p-type guard ring.

CELL SIZE: 150 BY 190 micrometer

CELL PLACEMENT: Outer p-type guard ring can overlap with other cell guard rings.

LAYOUT:



ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING DEPARTMENT

N-WELL BIPOLAR INTEGRATED CIRCUIT DESIGN MANUAL

CELL NAME: NWELL_XXXOHMB.CIF

DESCRIPTION:

These are base level resistors with three types of layouts and isolated by an N-well

CELL SIZE: 280 x 90, 360 x 90, 390 x 90, 440 x 90, 530 x 90, 810 x 90, 380 x 130, 1090 x 90, 470 x 130, 550 x 210

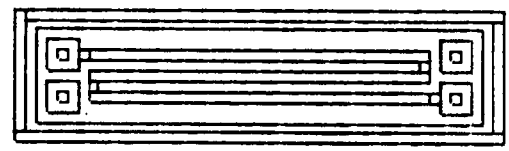
CELL PLACEMENT:

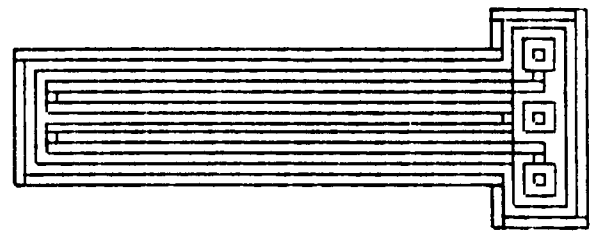
OTHER INFORMATION:

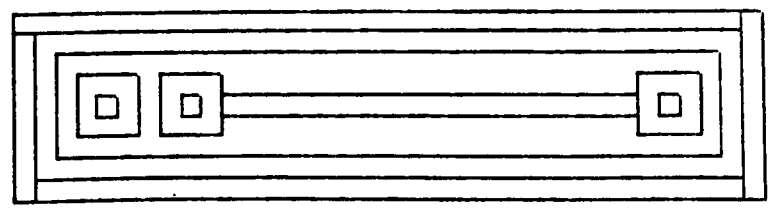
Resistor values are 3500, 5k, 6k, 7k, 9500, 16k, 18k, 22k, 25k, and 46500 ohms in order of cell geometry sizes. The XXX in cellname is replaced with verbatim resistor value.

SCHEMATIC

LAYOUT







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MICROELECTRONIC ENGINEERING DEPARTMENT

N-WELL BIPOLAR INTEGRATED CIRCUIT DESIGN MANUAL

CELL NAME: NWELL_XXXOHME.CIF

DESCRIPTION:

These are emitter level resistors

CELL SIZE: 50 x 70 um, 90 x 40 um, 130 x 30 um, 200 x 30 um, 330 x30 um

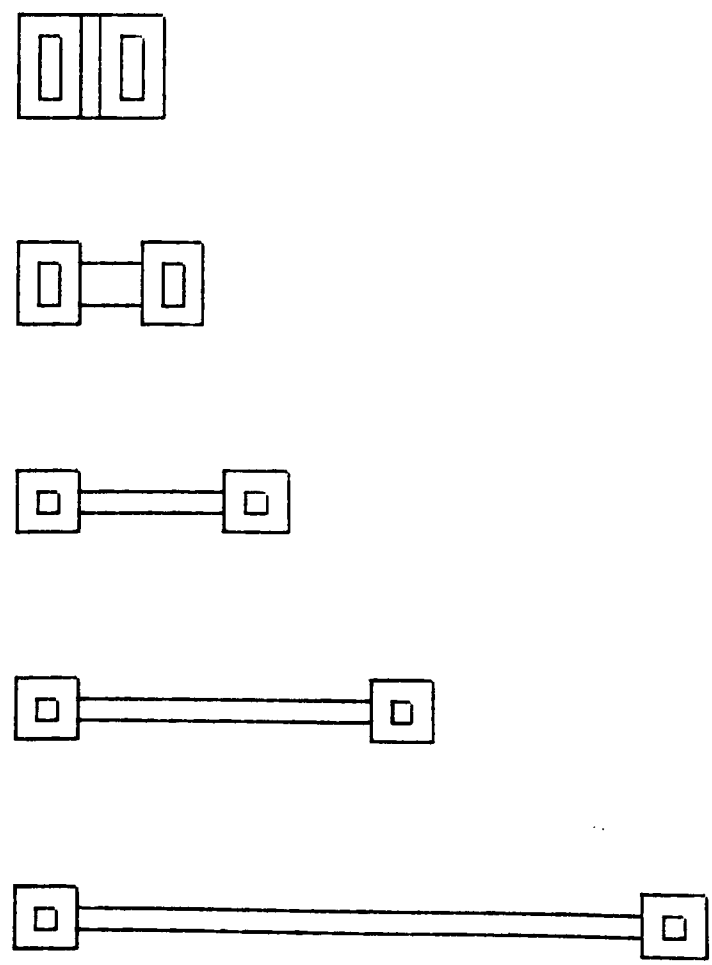
CELL PLACEMENT:

OTHER INFORMATION:

Values are 1, 10, 50, 100, and 200 ohms. The values replace the XXX in the cell names.

SCHEMATIC

LAYOUT



ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING DEPARTMENT

N-WELL BIPOLAR INTEGRATED CIRCUIT DESIGN MANUAL

CELL NAME: NWELL_VERTPNP.CIF

DESCRIPTION:

This is a minimum geometry vertical PNP substrate transistor

CELL SIZE: 90 x 150 microns

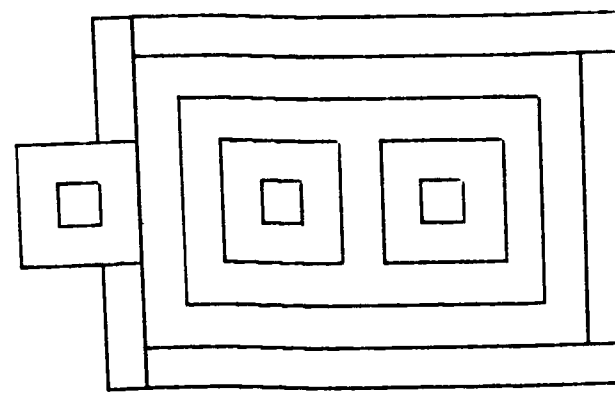
CELL PLACEMENT: The collector is the guardring. Collector voltage is always Vee voltage.

OTHER INFORMATION:

Beta=40, BVceo= >30 volts, Va >200 volts

SCHEMATIC

LAYOUT



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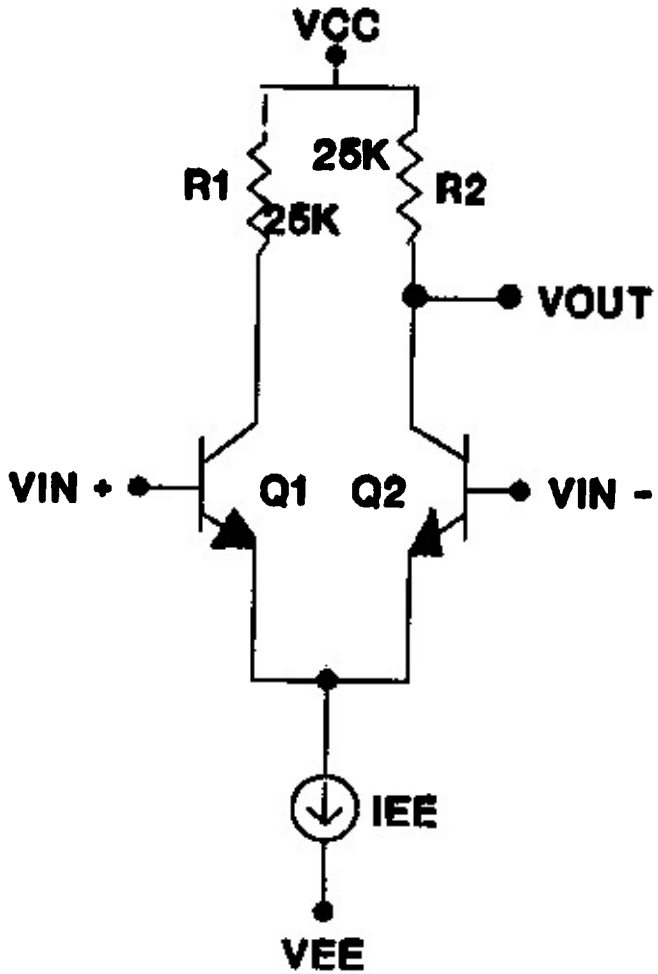
DEPARTMENT OF MICROELECTRONIC ENGINEERING
N-WELL BIPOLAR INTEGRATED CIRCUIT DESIGN MANUAL

DIFFERENTIAL AMPLIFIER DESIGN EXAMPLE

FOR THE

RIT N-WELL BIPOLAR PROCESS


VCC
R1
25K
25K
R2
VOUT
VIN +
Q1
Q2
VIN -
IEE
VEE

```
********18-JAN-91 *******  SPICE 2G.5 (10AUG81)  *******14:27:03*****

*  E DIFFAMP CHARACTERISTICS

****      INPUT LISTING                          TEMPERATURE =    27.000 DEG C

******************************************************************************


* A. LA PIETRA 8/17/90
* RIT N-WELL BIPOLAR
*
Q1 2 3 4 MOD1
Q2 7 0 6 MOD1
Q3 8 8 9 MOD1
Q4 5 8 9 MOD1
Q5 1 1 10 MOD1
Q6 11 11 12 MOD1
Q7 12 12 13 MOD1
Q8 13 8 9 MOD1
Q9 1 11 14 MOD1
Q10 14 13 9 MOD1
.MODEL MOD1 NPN IS=5.8649E-14 NF=1.0639 ISE=5.125E-14 NE=1.591
+   =160 VAF=75 RC=2E3 RE=8.0 IKF=.8E-3 VJE=.987 VJC=.753
+(  3=.662 TF=.336E-9
VCC 1 0 5
VEE 9 0 -5
VIN 3 0
RC1 1 2 25K
RC2 1 7 25K
RE1 4 5 10K
RE2 6 5 10K
RB 1 8 46.5K
RS 10 11 5.5K
RL 14 0 8.33K
.DC VIN -5 5 .5
.PRINT DC V(7)
.PLOT DC V(7)
.WIDTH OUT=80
.END
```

******16-JAN-91 ******* SPICE 2G.5 (10AUG81) *******14:27:03*****

: DIFFAMP CHARACTERISTICS

*** BJT MODEL PARAMETERS TEMPERATURE = 27.000 DEG C

****

	MOD1
YPE	NPN
S	5.86D-14
F	160.000
F	1.064
AF	7.50D+01
KF	8.00D-04
	5.12D-14
E	1.591
R	1.000
R	1.000
E	8.000
C	2000.000
JE	0.987
F	3.36D-10
JC	0.753
JS	0.662

******18-JAN-91 ******* SPICE 2G.5 (10AUG81) *******14:27:03*****

DIFFAMP CHARACTERISTICS

*** DC TRANSFER CURVES TEMPERATURE = 27.000 DEG C

****

VIN	V(7)
5.000E+00	1.149E-02
4.500E+00	1.149E-02
4.000E+00	1.149E-02
3.500E+00	1.149E-02
-3.000E+00	1.149E-02
-2.500E+00	1.149E-02
-2.000E+00	1.530E-01
-1.500E+00	7.044E-01
-1.000E+00	1.287E+00
-5.000E-01	1.877E+00
0.000E+00	2.469E+00
5.000E-01	3.062E+00
1.000E+00	3.653E+00
1.500E+00	4.234E+00
2.000E+00	4.791E+00
2.500E+00	5.000E+00
3.000E+00	5.000E+00
3.500E+00	5.000E+00
4.000E+00	5.000E+00
4.500E+00	5.000E+00
5.000E+00	5.000E+00

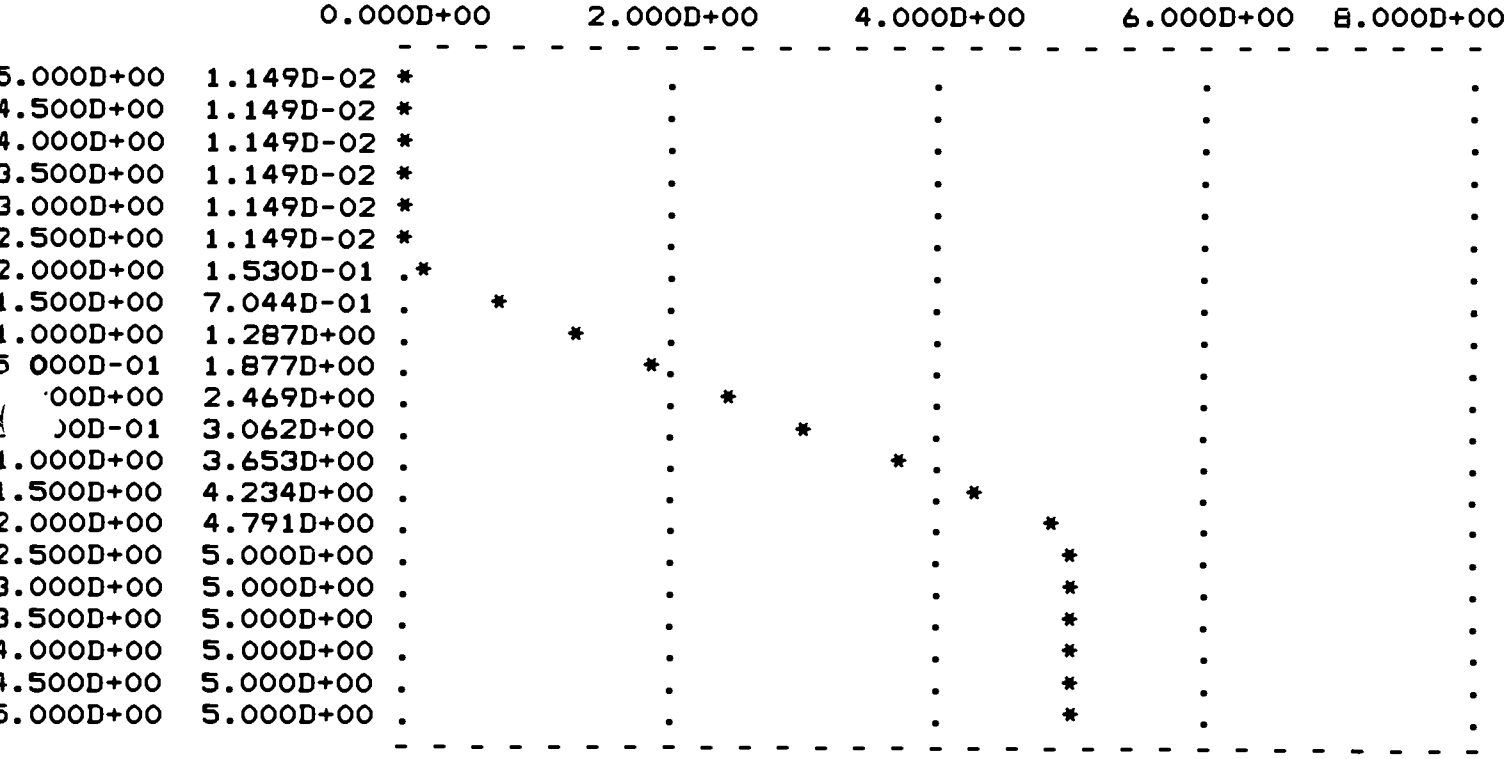
******18-JAN-91 ******* SPICE 2G.5 (10AUG81) *******14:27:03*****

DIFFAMP CHARACTERISTICS

*** DC TRANSFER CURVES TEMPERATURE = 27.000 DEG C

****

VIN V(7)

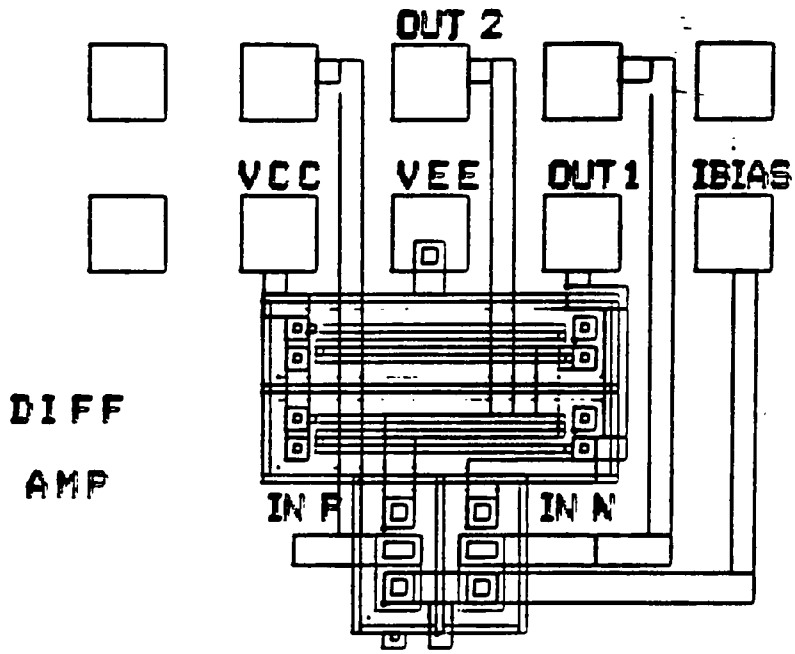


5.000D+00	1.149D-02
4.500D+00	1.149D-02
4.000D+00	1.149D-02
3.500D+00	1.149D-02
3.000D+00	1.149D-02
2.500D+00	1.149D-02
2.000D+00	1.530D-01
1.500D+00	7.044D-01
1.000D+00	1.287D+00
5 000D-01	1.877D+00
00D+00	2.469D+00
00D-01	3.062D+00
1.000D+00	3.653D+00
1.500D+00	4.234D+00
2.000D+00	4.791D+00
2.500D+00	5.000D+00
3.000D+00	5.000D+00
3.500D+00	5.000D+00
4.000D+00	5.000D+00
4.500D+00	5.000D+00
5.000D+00	5.000D+00

JOB CONCLUDED

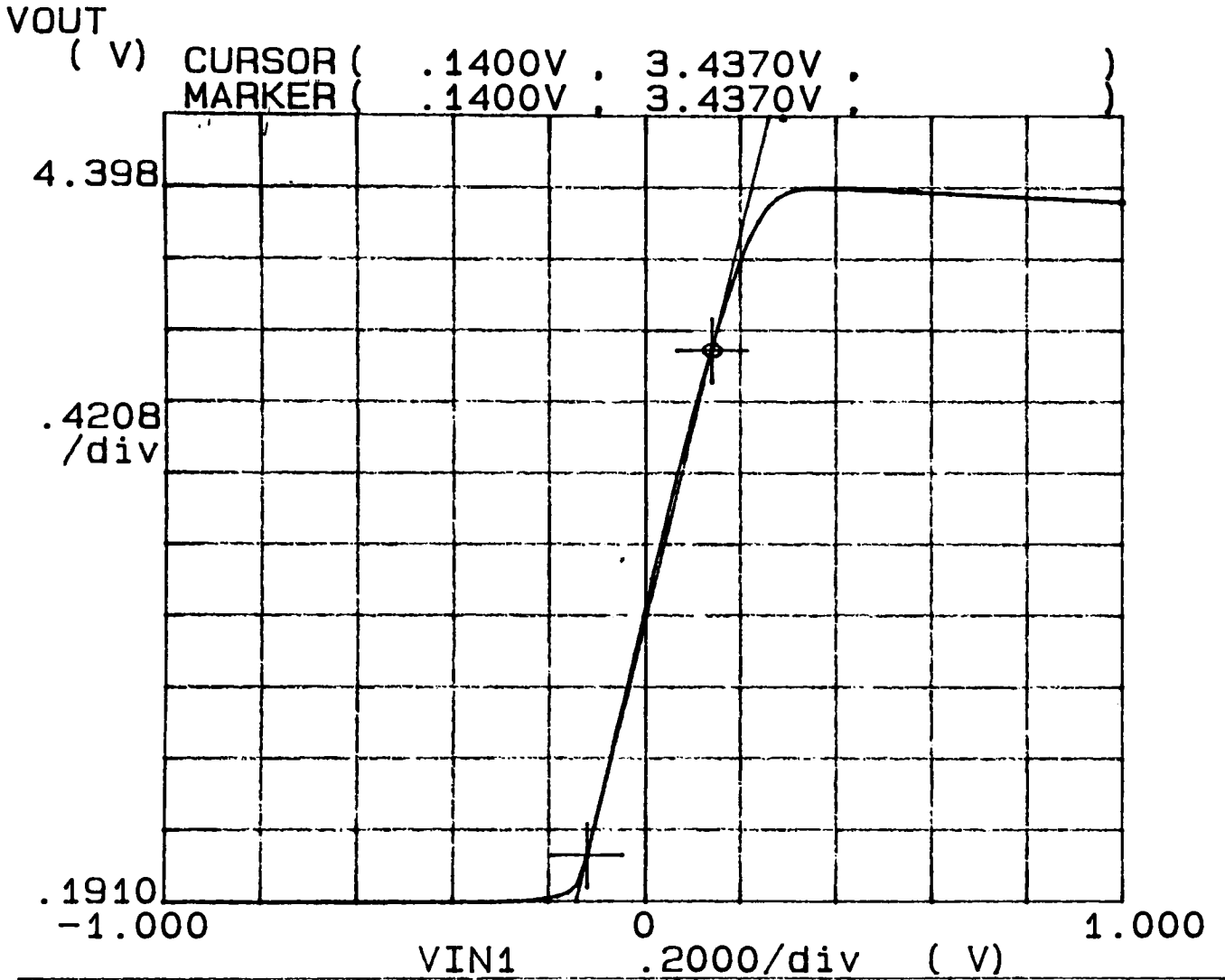
TIME		PAGE	DIRECT	BUFFERED
CPU	ELAPSED	FAULTS	I/O	I/O
0: 0.98	0: 0: 3.09	214	10	1

TOTAL JOB TIME 0.98


OUT 2
VCC
VEE
OUT 1
IBIAS
DIFF
AMP
IN P
IN N

****** GRAPHICS PLOT ******

DIFF AMP D5 10-24-90 ARL



Variable1:
VIN1 -Ch1
Linear sweep
Start -1.0000V
Stop 1.0000V
Step .0200V

Variable2:
IOUT -Ch3
Start .000 A
Stop .000 A
Step 40.00nA

Constants:
VIN2 -Ch2 .0000V
IBIAS -Ch4 -400.0uA
VCC -Vs1 5.0000V

	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	11.5E+00	87.3E-03	-160E-03	1.83E+00
LINE2				

ROCHESTER INSTITUTE OF TECHNOLOGY
DEPARTMENT OF MICROELECTRONIC ENGINEERING
N-WELL BIPOLAR INTEGRATED CIRCUIT DESIGN MANUAL

SUPREM SIMULATIONS

FOR THE

RIT N-WELL BIPOLAR PROCESS

```
**********************************************************
***                      SUPREM-3                      ***
***              Version C, Revision 8920              ***
***   Copyright (C) 1984,1985,1986,1987,1988,1989      ***
***       Technology Modeling Associates, Inc.         ***
***                 All Rights Reserved                ***
**********************************************************

                      3-DEC-90 10:42:14

  Statements input from file min30.in


 1... Title            RIT N-well Bipolar Electrical Simulation
 2... Comment                Andrew La Pietra

 3... $                Initialize the silicon substrate.
 4... Initialize       <100> silicon Boron=3e15
  ... +                Thickness=10.  dX=.075  XdX=.75 Spaces=100

 5... Comment          Field Oxide for implant
  .. Diffusion         Temperature=1100 Time=25  Wet02
(
 7... Comment          Etch windows in oxide for implant
 8... Etch             Oxide

 9... Comment          Implant and drive-in the Phosphorous layer.
10... Implant          Phosphor  Dose=8e12  Energy=110
11... Diffusion        Temperature=1150  Time=480  Dry02
12... Diffusion        Temperature=1150  Time=2400
13... $Print            Layer
14... $Plot             Chemical

15... Comment          Etch off the oxide formed during implant
16... Etch             Oxide

17... Comment          Boron Predepostion for base
18... Diffusion        Temperature=800  Time=30  t.rate=5.0  SS.Boron

19... Comment          Boron Predepostion for base
20... Diffusion        Temperature=950  Time=35  t.rate=0.0  SS.Boron

21... Comment          Boron Predepostion for base
22... Diffusion        Temperature=950  Time=30  t.rate=-5.0  SS.Boron

23... Comment          This is the LTO step to reduce base diffusion damage
 .. Diffusion          Temperature=750  Time=25 Wet02
(
25... Comment          Removal of BSG
26... Etch             Oxide

27... Comment          Boron Drive-in plus field oxidation for phos. diff
28... Diffusion        Temperature=1150  Time=30  Wet02
29..                   Temperature=1150  Time=30  Dry02
```

```
30.
31... Etch              Oxide

32... Comment           Phos. Predepostion for emitter
33... Diffusion         Temperature=800  Time=30  t.rate=5.0 SS.phosp

34... Comment           Phos. Predepostion for emitter
35... Diffusion         Temperature=950  Time=30  t.rate=0.0  SS.phosp

36... Comment           Phos. Predepostion for emitter
37... Diffusion         Temperature=950  Time=30  t.rate=-5.0 SS.phosp

38... Comment           Removal of PSG
39... Etch              Oxide

40... Comment           Phos. drive-in and CC mask
41... Diffusion         Temperature=1050  Time=20  WetO2

42... Comment           CC opening
43... Etch              Oxide

44... Print             Layers
45... Plot              Chemical Active boron phosphorous bottom=1E15
  ... +                 top=1E20
46... Plot              Chemical Active boron phosphorous bottom=1E15
  ... +                 top=1E20 Device=hp7550

47... Savefile          Structure File=fourelec.in
48... Stop

Input line #   4
Coefficient data group read
F  : S3COF0
D  :  1-AUG-90 18:54:43
Documentation from data file:

SUPREM-3 Revision 8920 coefficient initialization


Warning number   45 detected in line number  24
The temperature specified was less than 800 degrees Celsius.
The default diffusion and oxidation coefficients are not reliable
below this temperature.

Warning number  216 detected in line number  39
The top layer of the structure does not contain the material for
which an etch was specified. No etch has been performed.
```

N-well Bipolar Electrical Simulation
Opening

Material layer information
Input line # 44

layer no.	material	thickness (um)	dx (um)	xdx (um)	top node	bottom node	orientation or grain size
1	silicon	9.2212	0.0750	0.00	409	500	<100>

Integrated Dopant (#/cm**2)

layer	Net		Sum	
no.	active	chemical	active	chemical
1	4.9941E+15	5.6885E+15	5.1995E+15	5.8939E+15
sum	4.9941E+15	5.6885E+15	5.1995E+15	5.8939E+15

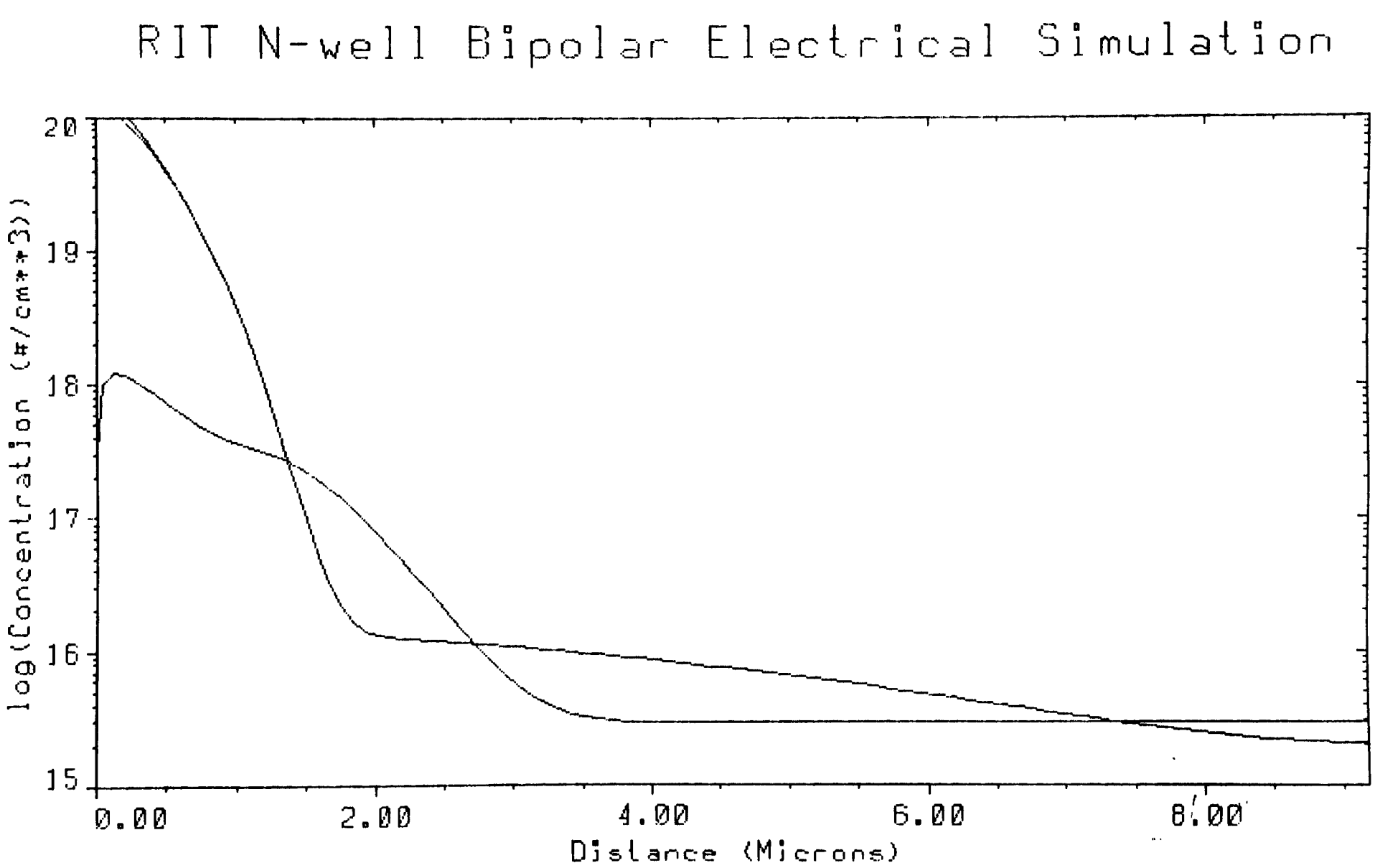
Integrated Dopant (#/cm**2)

layer	boron		phosphorus	
no.	active	chemical	active	chemical
1	1.0269E+14	1.0269E+14	5.0968E+15	5.7912E+15
sum	1.0269E+14	1.0269E+14	5.0968E+15	5.7912E+15

Boundary Locations and Integrated Dopant Concentrations for Each Diffused Region

layer no.	region no.	type	top depth (um)	bottom depth (um)	net active Qd (#/cm**2)	sum chemical Qd (#/cm**2)
1	4	n	0.0000	1.3888	5.0011E+15	5.8710E+15
1	3	p	1.3888	2.7244	8.3246E+12	1.7286E+13
1	2	n	2.7244	7.3505	1.5369E+12	4.6771E+12
1	1	p	7.3505	9.2212	1.1446E+11	9.9908E+11

*** END SUPREM-3 ***


RIT N-well Bipolar Electrical Simulation
20
19
18
17
16
15
log(Concentration (#/cm**3))
0.00
2.00
4.00
6.00
8.00
Distance (Microns)

ROCHESTER INSTITUTE OF TECHNOLOGY
DEPARTMENT OF MICROELECTRONIC ENGINEERING
N-WELL BIPOLAR INTEGRATED CIRCUIT DESIGN MANUAL

FACTORY SEQUENCE AND PROCESS STEP LIST

FOR THE

RIT N-WELL BIPOLAR PROCESS

ROCHESTER INSTITUTE OF TECHNOLOGY

MICROELECTRONIC ENGINEERING DEPARTMENT

QUALIFIED OPERATIONS LIBRARY

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OP. CODE	DESCRIPTION	Required Information
BNACT	P Type Planar Source Diffusion - Activation	
CLE01	MTI Scrub and RCA Clean	
CLE02	RCA Clean	
CVD01	Polysilicon Deposition	
DET01	4-pt. Probe Test of Diffused Layers on Step Etched Wafer	
DET02	4-pt. Probe Test of Diffused Layers on Control Wafer	
DIF01	P Type Diffusion (Predep. 1100 C, 13 min.)	
DIF01B	P Type Diffusion (Predep. 1000 C, 20 min.)	
DIF02	P Type Diffusion and Quick Oxide Growth (source= boron B-150)	Time and Temp.
DIF03	N Type Planar Source Diffusion- Predeposit	Time and Temp.
DIF04	P Type Planar Source Diffusion-	Time and Temp.
ETC01	Control Wafer Step Etch	Aprox. Oxide thickness
ETC02	Oxide Etch until Pull Dry	Aprox. oxide thickness
ETC03	Diff., Thin ox., or C.C. Oxide Etch	ETC (01 or 02) Data
ETC04	Paint Resist Stripes on a Step-Etched Wafer	
ETC05	Aluminum Etch	
ETC06	Oxide Etch w/out Resist Removal	
ETC07	Resist Strip	
ETC08	Plasma Etching of Polysilicon	
ETC09	Plasma Etching of Silicon Nitride	
GRV01	Groove and Stain for Junction Depth	
HOLD	Engineering Hold Step	
IDN01	Wafer ID Scribing, and 4-pt. Probe	Orient., Type, Resistivity
IMP01	Dopant Implantation	
MAS01	Create paper tape of MANN file	Name and loc. of MANN file
MAS02	Generation of reticle on MANN Pattern Generator	Name of MANN file
MAS03	Generation of Mask on Photorepeater, with RIT	Name Mann file and lay. name

	test die stepped in	
MAS04	Generation of Mask on Photorepeater, w/out RIT test die stepped in	Name Mann file and lay. name
MET01	Al Evaporation Deposition	Number of Pellets
NANO	Film Thickness Measurement	
OXI01	Wet Oxide - 5000 Angstroms	
OXI02	Dry Oxide - 600 Angstroms	
OXI03	Dry Oxide - 600 Angstroms and Anneal	
OXI04	Wet Oxide	Time, Temp, 02 Flow Rate and Approximate Thickness
OXI05	Dry Oxide and Anneal	Time, Temp, 02 Flow Rate and Approximate Thickness
OXI06	Dry Oxide and Anneal using TCA Gettering	Time, Temp, 02 Flow Rate and Approximate Thickness
OXI08	Post Implant Anneal	Time, Temp, 02 Flow Rate and Approximate Thickness
PATGEN	Generation of reticle on MANN 3000 Pattern Generator	
PHACT	N Type Planar Source Diffusion - Activation	
PHL01	Kodak 820 Resist Coat and Exposure.	Mask Number and Name
PHL02	Kodak 820 Resist Coat and and Exposure for Metal Patterning.	Mask Number and Name
PHL03	KTI-820 Resist Coat and Exposure (GCA Stepper)	Mask Number and Name
PIM01	Polyimide Processing	
SIN01	Wafer Sinter	
TES01	Parameter Analyzer Testing of Fabricated Devices	

Operation Code Key

CLE - Cleaning
DIF - Diffusion
END - Finished
ENG - Engineering Request
ETC - Etch Oxide and Metal
IDN - Identification Step
MAS - Mask Making
MET - Metallization
OXI - Oxide
PHL - Photolithography
SIN - Sintering
TES - Testing

ROCHESTER INSTITUTE OF TECHNOLOGY
DEPARTMENT OF MICROELECTRONIC ENGINEERING
ESTABLISHING AN N-WELL BIPOLAR FABRICATION SERVICE AT RIT

APPENDIX 4.2

OPERATIONAL AMPLIFIER

DC AND AC SPICE SIMULATIONS

3 OPAMP CHARACTERISTICS

** INPUT LISTING TEMPERATURE = 27.000 DEG C

****

```
A. LA PIETRA 8/17/90
RIT N-WELL BIPOLAR
 2 3 6 MOD1
 5 0 6 MOD1
 1 2 7 MOD1
 9 8 10 MOD1
 11 15 10 MOD1
 10 12 13 MOD1
 8 12 13 MOD1
 6 12 13 MOD1
 12 12 13 MOD1
0 1 5 14 MOD1
1 15 12 13 MOD1
2 1 9 16 MOD1
3 17 17 18 MOD1
  18 18 19 MOD1
  19 12 13 MOD1
6 1 17 20 MOD1
7 13 19 20 MOD2
ODEL MOD1 NPN IS=5.8649E-14 NF=1.0639 ISE=5.125E-14 NE=1.591
BF=160 VAF=75 RC=2E3 RE=8.0 IKF=.8E-3 VJE=.987 VJC=.753 RB=585
VJS=.662 TF=.336E-9 CJS=2.9629E-12 CJC=1.7201E-12 CJE=1.4711E-12
ODEL MOD2 PNP BF=40 VA=100 RC=2.5K CJE=1.7201E-12 CJC=2.9629E-12
RC=2E3
C 1 0 5
E 13 0 -5
N 3 0
1 1 2 25K
2 1 5 25K
3 1 9 25K
4 1 11 25K
IAS 1 12 46.5K
1 7 8 18K
2 14 15 18K
3 16 17 7K
PTIONS LIMPTS=5000
C VIN -.005 .005 .0005
LOT DC V(20)
IDTH OUT=80
ND
```

(2 OPAMP CHARACTERISTICS

*** BJT MODEL PARAMETERS TEMPERATURE = 27.000 DEG C

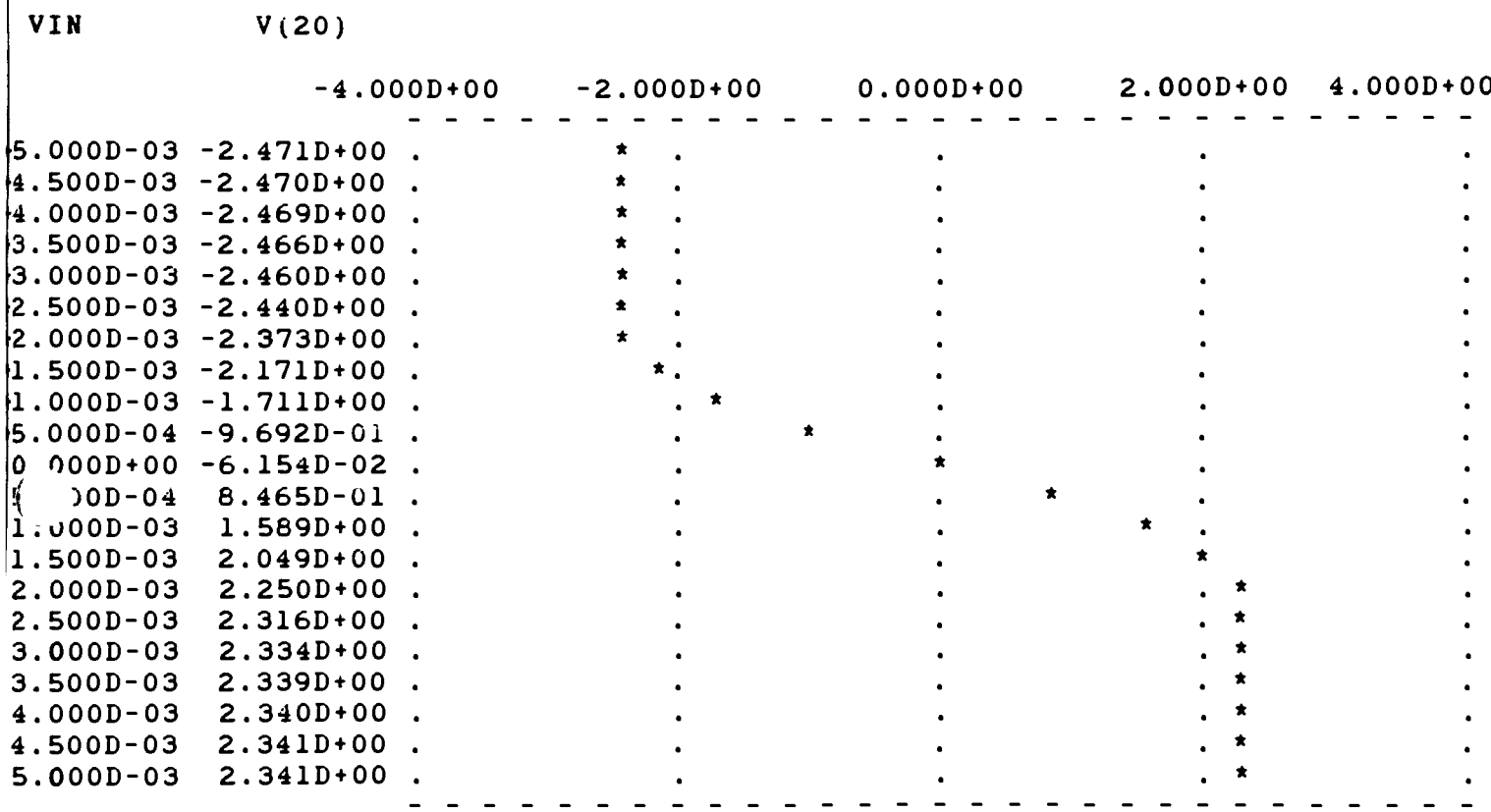
****

	MOD1	MOD2
YPE	NPN	PNP
S	5.86D-14	1.00D-16
F	160.000	40.000
F	1.064	1.000
AF	7.50D+01	1.00D+02
KF	8.00D-04	0.00D+00
S	5.12D-14	0.00D+00
E	1.591	1.500
R	1.000	1.000
R	1.000	1.000
B	585.000	0.000
E	8.000	0.000
C	2000.000	2000.000
JE	1.47D-12	1.72D-12
JE	0.987	0.750
F	3.36D-10	0.00D+00
JC	1.72D-12	2.96D-12
JC	0.753	0.750
JS	2.96D-12	0.00D+00
	0.662	0.750

E OPAMP CHARACTERISTICS

*** DC TRANSFER CURVES TEMPERATURE = 27.000 DEG C

****



JOB CONCLUDED

TIME		PAGE	DIRECT	BUFFERED
CPU	ELAPSED	FAULTS	I/O	I/O
0: 1.56	0: 0: 2.23	112	8	1

TOTAL JOB TIME 1.56

```
****** 2-JAN-91 *******  SPICE 2G.5 (10AUG81)  *******12:19:30*****

PICE OPAMP CHARACTERISTICS

        INPUT LISTING                          TEMPERATURE =   27.000 DEG C

******************************************************************************



 A. LA PIETRA 8/17/90
 RIT N-WELL BIPOLAR
 AC CHARACTERISTICS - COMPENSATION
Q1 2 3 6 MOD1
Q2 5 0 6 MOD1
Q3 1 2 7 MOD1
Q4 9 8 10 MOD1
Q5 11 15 10 MOD1
Q6 10 12 13 MOD1
Q7 8 12 13 MOD1
Q8 6 12 13 MOD1
Q9 12 12 13 MOD1
Q10 1 5 14 MOD1
Q11 15 12 13 MOD1
Q12 1 9 16 MOD1
Q13 17 17 18 MOD1
Q14 18 18 19 MOD1
Q15 19 12 13 MOD1
Q?   1 17 20 MOD1
Q1   13 19 20 MOD2
.MODEL MOD1 NPN IS=5.8649E-14 NF=1.0639 ISE=5.125E-14 NE=1.591
+ BF=160 VAF=75 RC=2E3 RE=8.0 IKF=.8E-3 VJE=.987 VJC=.753 RB=585
+ VJS=.662 TF=.336E-9 CJS=2.9629E-12 CJC=1.7201E-12 CJE=1.4711E-12
.MODEL MOD2 PNP BF=40 VA=100 RC=2.5K CJE=1.7201E-12 CJC=2.9629E-12
+ RC=2E3
VCC 1 0 5
VEE 13 0 -5
VIN 3 0 AC 5
RC1 1 2 25K
RC2 1 5 25K
RC3 1 9 25K
RC4 1 11 25K
RBIAS 1 12 46.5K
RS1 7 8 18K
RS2 14 15 18K
RS3 16 17 7K
CCOMP1 2 9 310E-12
.AC DEC 10 1 100MEG
.OPTIONS LIMPTS=5000
.PRINT AC VDB(15) VP(15)
.PLOT AC VDB(15) VP(15)
.WIDTH OUT=80
.END
```

PICE OPAMP CHARACTERISTICS

BJT MODEL PARAMETERS TEMPERATURE = 27.000 DEG C

****

	MOD1	MOD2
YPE	NPN	PNP
S	5.86D-14	1.00D-16
F	160.000	40.000
NF	1.064	1.000
AF	7.50D+01	1.00D+02
KF	8.00D-04	0.00D+00
SE	5.12D-14	0.00D+00
NE	1.591	1.500
BR	1.000	1.000
NR	1.000	1.000
RB	585.000	0.000
RE	8.000	0.000
RC	2000.000	2000.000
CJE	1.47D-12	1.72D-12
VJE	0.987	0.750
TF	3.36D-10	0.00D+00
CJC	1.72D-12	2.96D-12
VJC	0.753	0.750
CJS	2.96D-12	0.00D+00
VJS	0.662	0.750

****** 2-JAN-91 ******* SPICE 2G.5 (10AUG81) *******12:19:30*****

PICE OPAMP CHARACTERISTICS

SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C

****

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
1)	5.0000	(2)	2.4532	(3)	0.0000	(5)	2.4532
6)	-0.5886	(7)	1.8417	(8)	-1.7561	(9)	2.5063
10)	-2.3433	(11)	2.5462	(12)	-4.3884	(13)	-5.0000
14)	1.8417	(15)	-1.7561	(16)	1.8945	(17)	0.4860
18)	-0.1270	(19)	-0.7400	(20)	-0.0615		

VOLTAGE SOURCE CURRENTS

NAME	CURRENT
VCC	-1.226D-03
VEE	1.227D-03
VIN	-7.632D-07

TOTAL POWER DISSIPATION 1.23D-02 WATTS

PICE OPAMP CHARACTERISTICS

OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

****

*** BIPOLAR JUNCTION TRANSISTORS

	Q1	Q2	Q3	Q4	Q5	Q6	Q7
ODEL	MOD1	MOD1	MOD1	MOD1	MOD1	MOD1	MOD1
IB	7.63E-07	7.63E-07	1.63E-06	7.28E-07	7.28E-07	1.64E-06	1.64E-06
IC	1.00E-04	1.00E-04	1.98E-04	9.81E-05	9.81E-05	1.98E-04	1.99E-04
VBE	0.589	0.589	0.611	0.587	0.587	0.612	0.612
VBC	-2.453	-2.453	-2.547	-4.262	-4.302	-2.045	-2.632
VCE	3.042	3.042	3.158	4.850	4.890	2.657	3.244
BETADC	131.344	131.344	121.514	134.830	134.898	120.655	121.581
GM	3.28E-03	3.28E-03	6.03E-03	3.23E-03	3.23E-03	6.01E-03	6.06E-03
RPI	3.74E+04	3.74E+04	1.73E+04	3.92E+04	3.92E+04	1.73E+04	1.73E+04
RX	5.85E+02	5.85E+02	5.85E+02	5.85E+02	5.85E+02	5.85E+02	5.85E+02
RO	7.71E+05	7.71E+05	3.89E+05	8.06E+05	8.06E+05	3.88E+05	3.88E+05
CPI	3.07E-12	3.07E-12	4.02E-12	3.05E-12	3.05E-12	4.01E-12	4.03E-12
CMU	1.09E-12	1.09E-12	1.10E-12	9.32E-13	9.30E-13	1.17E-12	1.09E-12
CBX	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
CCS	2.96E-12	2.96E-12	2.96E-12	2.96E-12	2.96E-12	2.96E-12	2.96E-12
BETAAC	122.763	122.763	104.624	126.575	126.639	103.828	104.630
FT	1.26E+08	1.26E+08	1.87E+08	1.29E+08	1.29E+08	1.85E+08	1.88E+08

	Q8	Q9	Q10	Q11	Q12	Q13	Q14
MODEL	MOD1	MOD1	MOD1	MOD1	MOD1	MOD1	MOD1
IB	1.64E-06	1.79E-06	1.63E-06	1.64E-06	1.65E-06	1.98E-06	1.98E-06
IC	2.02E-04	1.92E-04	1.98E-04	1.99E-04	2.00E-04	1.99E-04	1.99E-04
VBE	0.612	0.612	0.611	0.612	0.612	0.613	0.613
VBC	-3.800	0.000	-2.547	-2.632	-2.494	0.000	0.000
VCE	4.411	0.612	3.158	3.244	3.105	0.613	0.613
BETADC	123.422	107.025	121.514	121.581	121.270	100.414	100.414
GM	6.14E-03	5.84E-03	6.03E-03	6.06E-03	6.07E-03	6.03E-03	6.03E-03
RPI	1.73E+04	1.73E+04	1.73E+04	1.73E+04	1.72E+04	1.66E+04	1.66E+04
RX	5.85E+02	5.85E+02	5.85E+02	5.85E+02	5.85E+02	5.85E+02	5.85E+02
RO	3.88E+05	1.34E+05	3.89E+05	3.88E+05	3.86E+05	9.04E+04	9.04E+04
CPI	4.06E-12	3.96E-12	4.02E-12	4.03E-12	4.03E-12	4.02E-12	4.02E-12
CMU	9.79E-13	2.17E-12	1.10E-12	1.09E-12	1.11E-12	2.20E-12	2.20E-12
CBX	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
CCS	2.96E-12	2.96E-12	2.96E-12	2.96E-12	2.96E-12	2.96E-12	2.96E-12
BETAAC	106.225	101.038	104.624	104.630	104.295	99.813	99.813
FT	1.94E+08	1.52E+08	1.87E+08	1.88E+08	1.88E+08	1.54E+08	1.54E+08

	Q15	Q16	Q17

DEL			MOD2
	1.64E-06	1.89E-07	-6.17E-07
	2.02E-04	2.61E-05	-2.57E-05
E	0.612	0.548	-0.678
C	-3.648	-4.514	4.260
E	4.260	5.062	-4.938
T^DC	123.181	137.922	41.684
(	6.13E-03	9.22E-04	9.93E-04
1	1.73E+04	1.53E+05	4.20E+04
	5.85E+02	5.85E+02	0.00E+00
)	3.88E+05	3.04E+06	4.05E+06
I	4.05E-12	2.23E-12	2.74E-12
U	9.91E-13	9.08E-13	1.59E-12
X	0.00E+00	0.00E+00	0.00E+00
S	2.96E-12	2.96E-12	0.00E+00
TAAC	106.015	141.425	41.673
	1.93E+08	4.68E+07	3.65E+07

SPICE OPAMP CHARACTERISTICS

AC ANALYSIS TEMPERATURE = 27.000 DEG C

FREQ	VDB(15)	VP(15)
1.000E+00	4.206E+01	3.189E-02
1.259E+00	4.206E+01	4.015E-02
1.585E+00	4.206E+01	5.054E-02
1.995E+00	4.206E+01	6.363E-02
2.512E+00	4.206E+01	8.010E-02
3.162E+00	4.206E+01	1.008E-01
3.981E+00	4.206E+01	1.269E-01
5.012E+00	4.206E+01	1.598E-01
6.310E+00	4.206E+01	2.012E-01
7.943E+00	4.206E+01	2.533E-01
1.000E+01	4.206E+01	3.188E-01
1.259E+01	4.206E+01	4.013E-01
1.585E+01	4.206E+01	5.051E-01
1.995E+01	4.207E+01	6.356E-01
2.512E+01	4.207E+01	7.997E-01
[illegible]52E+01	4.207E+01	1.006E+00
[illegible]81E+01	4.207E+01	1.265E+00
5.012E+01	4.208E+01	1.588E+00
6.310E+01	4.209E+01	1.992E+00
7.943E+01	4.211E+01	2.494E+00
1.000E+02	4.214E+01	3.111E+00
1.259E+02	4.218E+01	3.862E+00
1.585E+02	4.224E+01	4.757E+00
1.995E+02	4.234E+01	5.790E+00
2.512E+02	4.248E+01	6.926E+00
3.162E+02	4.267E+01	8.084E+00
3.981E+02	4.293E+01	9.126E+00
5.012E+02	4.324E+01	9.878E+00
6.310E+02	4.359E+01	1.018E+01
7.943E+02	4.394E+01	9.952E+00
1.000E+03	4.426E+01	9.244E+00
1.259E+03	4.453E+01	8.197E+00
1.585E+03	4.474E+01	6.985E+00
1.995E+03	4.489E+01	5.755E+00
2.512E+03	4.500E+01	4.595E+00
3.162E+03	4.507E+01	3.548E+00
3.981E+03	4.512E+01	2.618E+00
5.012E+03	4.515E+01	1.788E+00
6.310E+03	4.517E+01	1.035E+00
7.943E+03	4.518E+01	3.261E-01
[illegible]00E+04	4.518E+01	-3.702E-01
[illegible]59E+04	4.519E+01	-1.089E+00
1.585E+04	4.519E+01	-1.867E+00
1.995E+04	4.519E+01	-2.744E+00
2.512E+04	4.519E+01	-3.768E+00
3.162E+04	4.518E+01	-4.991E+00
3.981E+04	4.517E+01	-6.478E+00
5.012E+04	4.515E+01	-8.307E+00
[illegible]	[illegible]	[illegible]

1.000E+05	4.501E+01	-1.687E+01
1.259E+05	4.491E+01	-2.121E+01
1.585E+05	4.474E+01	-2.656E+01
1.995E+05	4.449E+01	-3.311E+01
2.512E+05	4.411E+01	-4.104E+01
3.162E+05	4.355E+01	-5.049E+01
[illegible]31E+05	4.275E+01	-6.151E+01
5.012E+05	4.164E+01	-7.409E+01
6.310E+05	4.015E+01	-8.812E+01
7.943E+05	3.820E+01	-1.034E+02
1.000E+06	3.568E+01	-1.196E+02
1.259E+06	3.245E+01	-1.358E+02
1.585E+06	2.842E+01	-1.505E+02
1.995E+06	2.361E+01	-1.609E+02
2.512E+06	1.839E+01	-1.639E+02
3.162E+06	1.366E+01	-1.584E+02
3.981E+06	1.026E+01	-1.502E+02
5.012E+06	7.740E+00	-1.468E+02
6.310E+06	5.296E+00	-1.485E+02
7.943E+06	2.614E+00	-1.537E+02
1.000E+07	-4.107E-01	-1.613E+02
1.259E+07	-3.871E+00	-1.708E+02
1.585E+07	-7.882E+00	1.785E+02
1.995E+07	-1.257E+01	1.671E+02
2.512E+07	-1.814E+01	1.554E+02
3.162E+07	-2.519E+01	1.423E+02
3.981E+07	-3.651E+01	1.197E+02
5.012E+07	-4.112E+01	-2.910E+01
6.310E+07	-3.454E+01	-5.725E+01
7.943E+07	-3.324E+01	-7.326E+01
1.000E+08	-3.377E+01	-8.760E+01

******* 2-JAN-91 ******* SPICE 2G.5 (10AUG81) *******12:19:30*****

PICE OPAMP CHARACTERISTICS

AC ANALYSIS TEMPERATURE = 27.000 DEG C

****

EGEND:

: VDB(15)
: VP(15)

FREQ	VDB(15)	-1.000D+02	-5.000D+01	0.000D+00	5.000D+01	1.000D+02
		-2.000D+02	-1.000D+02	0.000D+00	1.000D+02	2.000D+02
1.000D+00	4.206D+01			+	*	
1.259D+00	4.206D+01			+	*	
1.585D+00	4.206D+01			+	*	
1.995D+00	4.206D+01			+	*	
2.512D+00	4.206D+01			+	*	
3.162D+00	4.206D+01			+	*	
3.981D+00	4.206D+01			+	*	
5.012D+00	4.206D+01			+	*	
6.310D+00	4.206D+01			+	*	
7.943D+00	4.206D+01			+	*	
1.000D+01	4.206D+01			+	*	
1.259D+01	4.206D+01			+	*	
1.585D+01	4.206D+01			+	*	
1.995D+01	4.207D+01			+	*	
2.512D+01	4.207D+01			+	*	
3.162D+01	4.207D+01			+	*	
3.981D+01	4.207D+01			+	*	
5.012D+01	4.208D+01			+	*	
6.310D+01	4.209D+01			+	*	
7.943D+01	4.211D+01			+	*	
1.000D+02	4.214D+01			+	*	
1.259D+02	4.218D+01			.+	*	
1.585D+02	4.224D+01			.+	*	
1.995D+02	4.234D+01			.+	*	
2.512D+02	4.248D+01			.+	*	
3.162D+02	4.267D+01			.+	*	
3.981D+02	4.293D+01			.+	*	
5.012D+02	4.324D+01			.+	*	
6.310D+02	4.359D+01			.+	*	
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1.000D+03	4.426D+01			.+	*	
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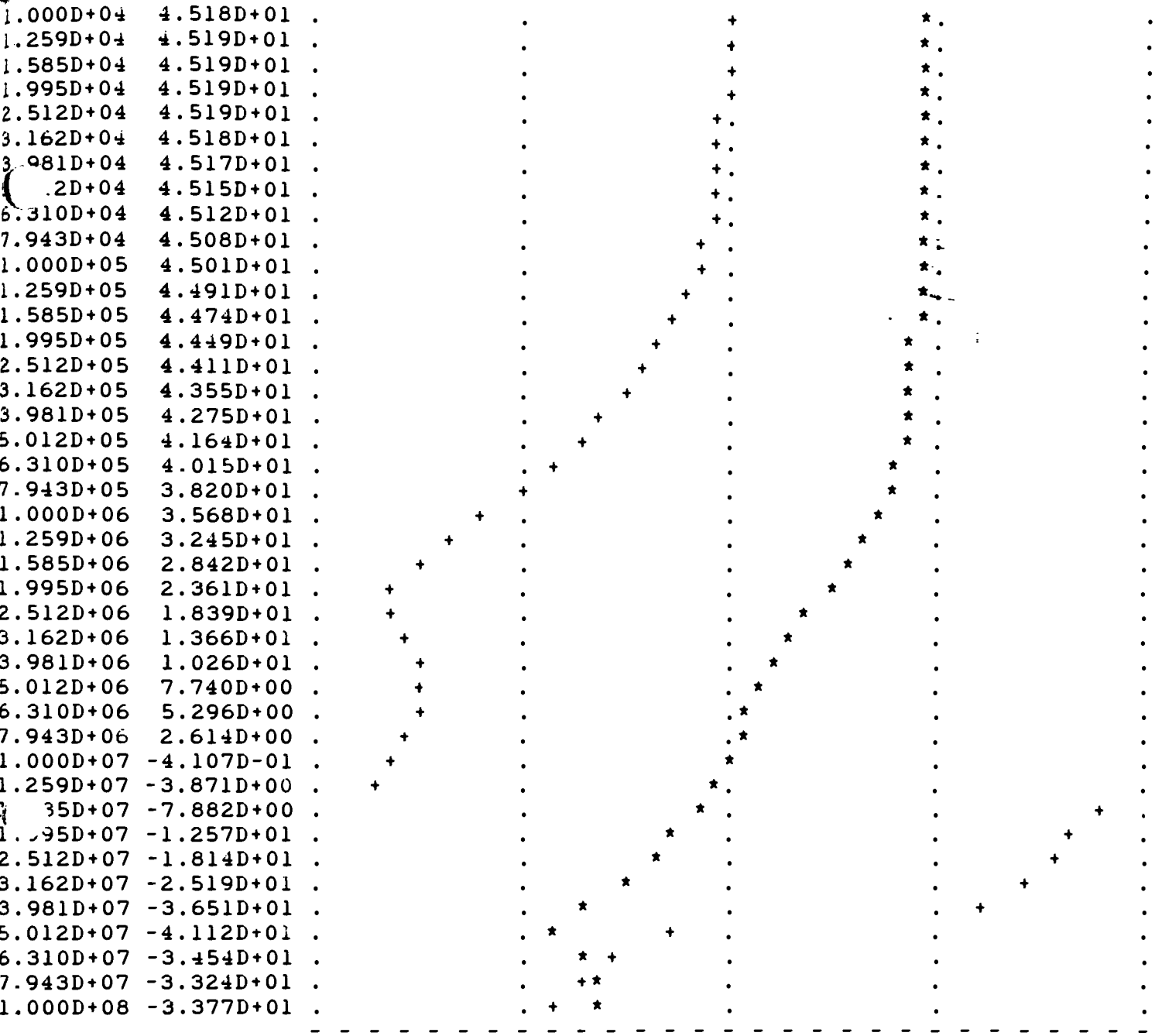

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1.585D+05	4.474D+01
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2.512D+05	4.411D+01
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7.943D+05	3.820D+01
1.000D+06	3.568D+01
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1.585D+06	2.842D+01
1.995D+06	2.361D+01
2.512D+06	1.839D+01
3.162D+06	1.366D+01
3.981D+06	1.026D+01
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JOB CONCLUDED

TIME		PAGE	DIRECT	BUFFERED
CPU	ELAPSED	FAULTS	I/O	I/O
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TOTAL JOB TIME 2.84

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